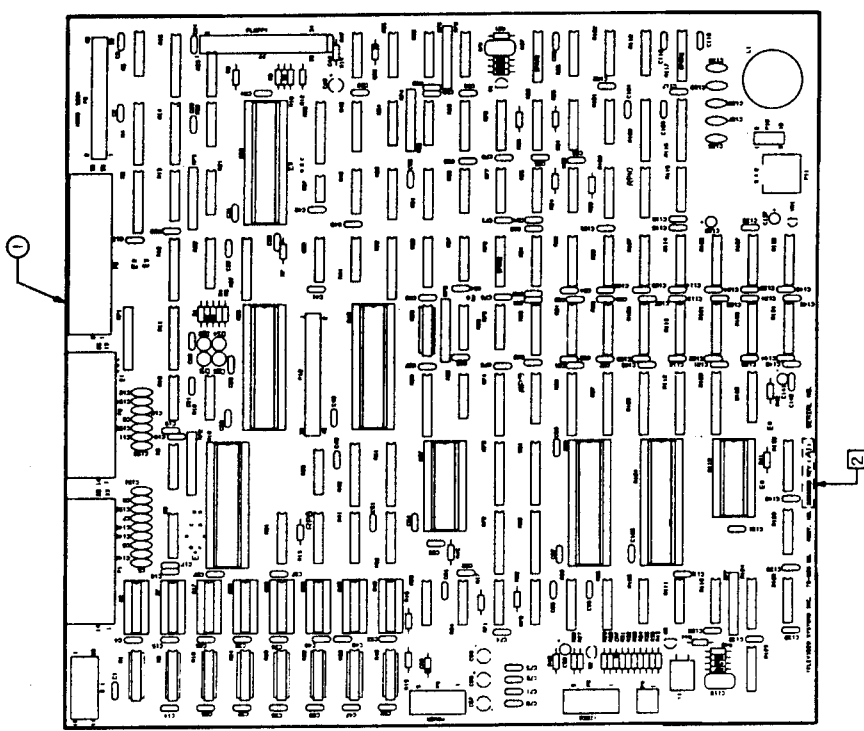


TELEVIDEO TS 803/803H SCHEMATICS.



- NOTE: UNLESS OTHERWISE SPECIFIED
1. COMPLETE HEIGHT NOT TO EXCEED .80 ABOVE MOUNTING SURFACE OF BOARD.
 2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50-100R APPROXIMATELY WHERE SHOWN.
 3. MADE FROM 222 G100. FAB REV A.
 4. ALL COMPONENT HOLES NOT TO BE PLUGGED UNLESS SPECIFIED. (FEED THRU'S ARE PLUGGED UNLESS SPECIFIED)

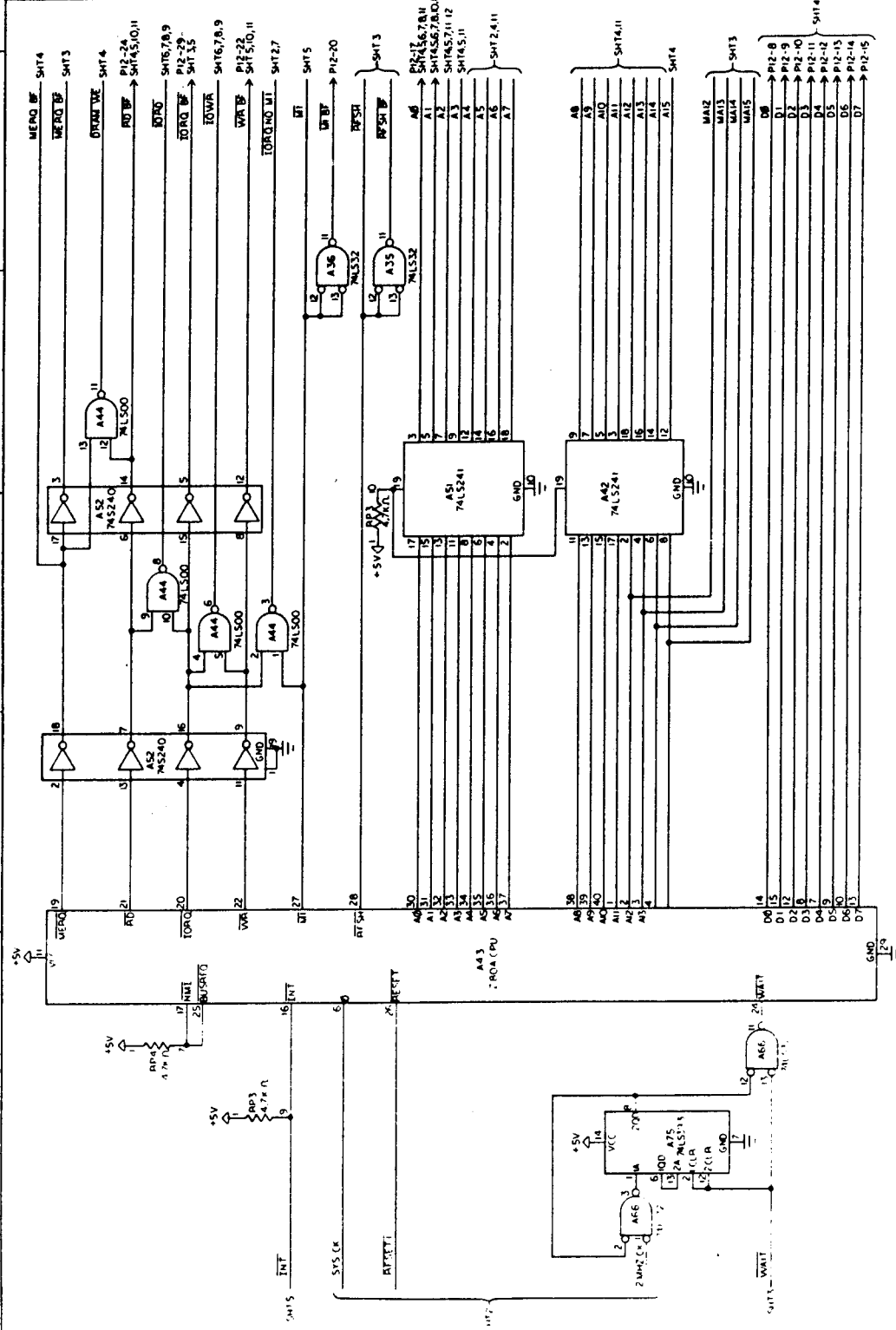
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A	1	PROD REL PER ECO 0641	7/2/83	JAL
A1	1	RECORD CHG PER ECO 0692	8/11/83	JAL

ZONE	LINE	REVISIONS	DATE	APPROVED
A	1	PROD REL PER ECO 0641	7/2/83	JAL
A1	1	RECORD CHG PER ECO 0692	8/11/83	JAL

TELEVIDEO, INC.
PCB ASSY DWG
TS 803 CMP BD

ZONE	LINE	REVISIONS	DATE	APPROVED
A	1	PROD REL PER ECO 0641	7/2/83	JAL
A1	1	RECORD CHG PER ECO 0692	8/11/83	JAL

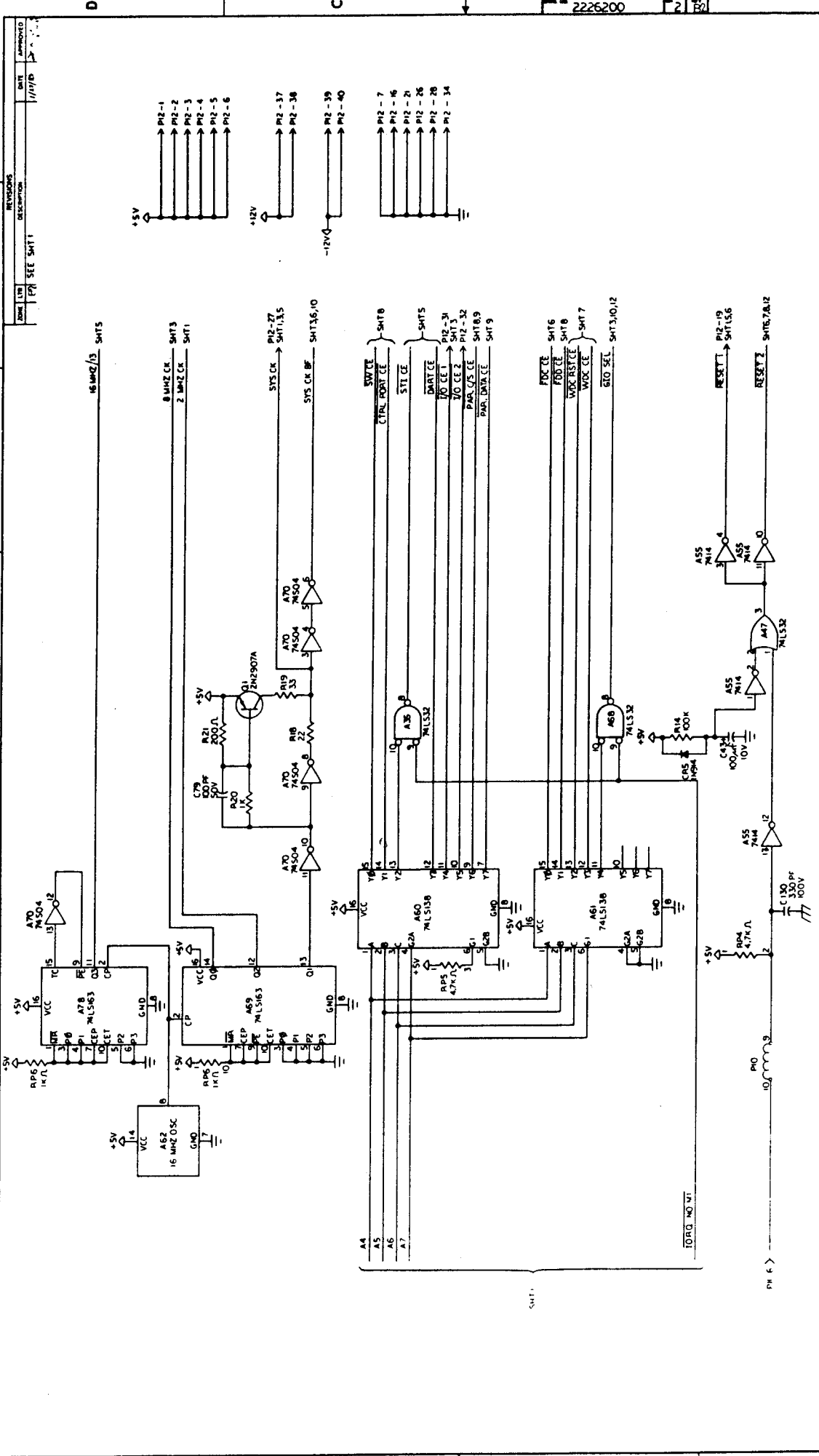
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B	1	INCORP PER ECO 0676	3/1/73	
B1	1	RECORD CHG PER ECO 0684	4/10/73	
B2	1		4/26/73	



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE VALUED IN OHMS
 AND ARE 1/4 WATT 5%.
 2. ALL CAPACITORS ARE VALUED IN UF
 AND ARE 16 VDC +10%.

DATE	1/21/73	REV	1
DESCRIPTION	PCB SCHEMATIC TS803 CMP BD		
DESIGNED BY	J. L. B. 10/1/72		
CHECKED BY	J. L. B. 10/1/72		
APPROVED BY	J. L. B. 10/1/72		
DATE	1/21/73	REV	1
DESCRIPTION	PCB SCHEMATIC TS803 CMP BD		
DESIGNED BY	J. L. B. 10/1/72		
CHECKED BY	J. L. B. 10/1/72		
APPROVED BY	J. L. B. 10/1/72		

THE INFORMATION CONTAINED HEREIN IS UNCLASSIFIED
 DATE 10/1/72 BY J. L. B. 10/1/72
 EXEMPT FROM GDSR, E.O. 12958, 1.4
 EXEMPT FROM GDSR, E.O. 12958, 1.4
 EXEMPT FROM GDSR, E.O. 12958, 1.4



REVISIONS		DATE	APPROVED
1	REVISED	11/11/82	
2	REVISED	11/11/82	
3	REVISED	11/11/82	
4	REVISED	11/11/82	
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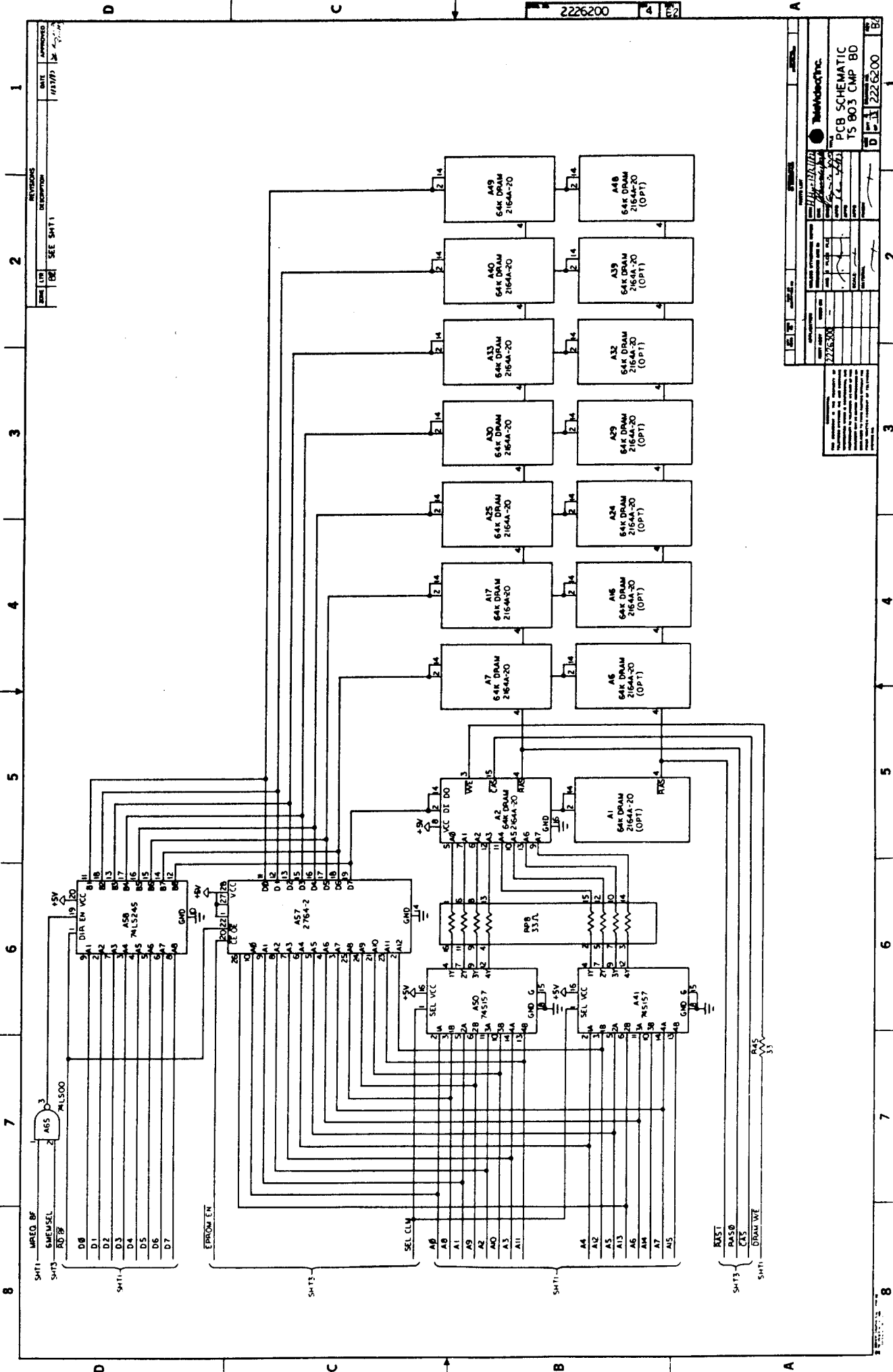
2226200

PCB SCHEMATIC

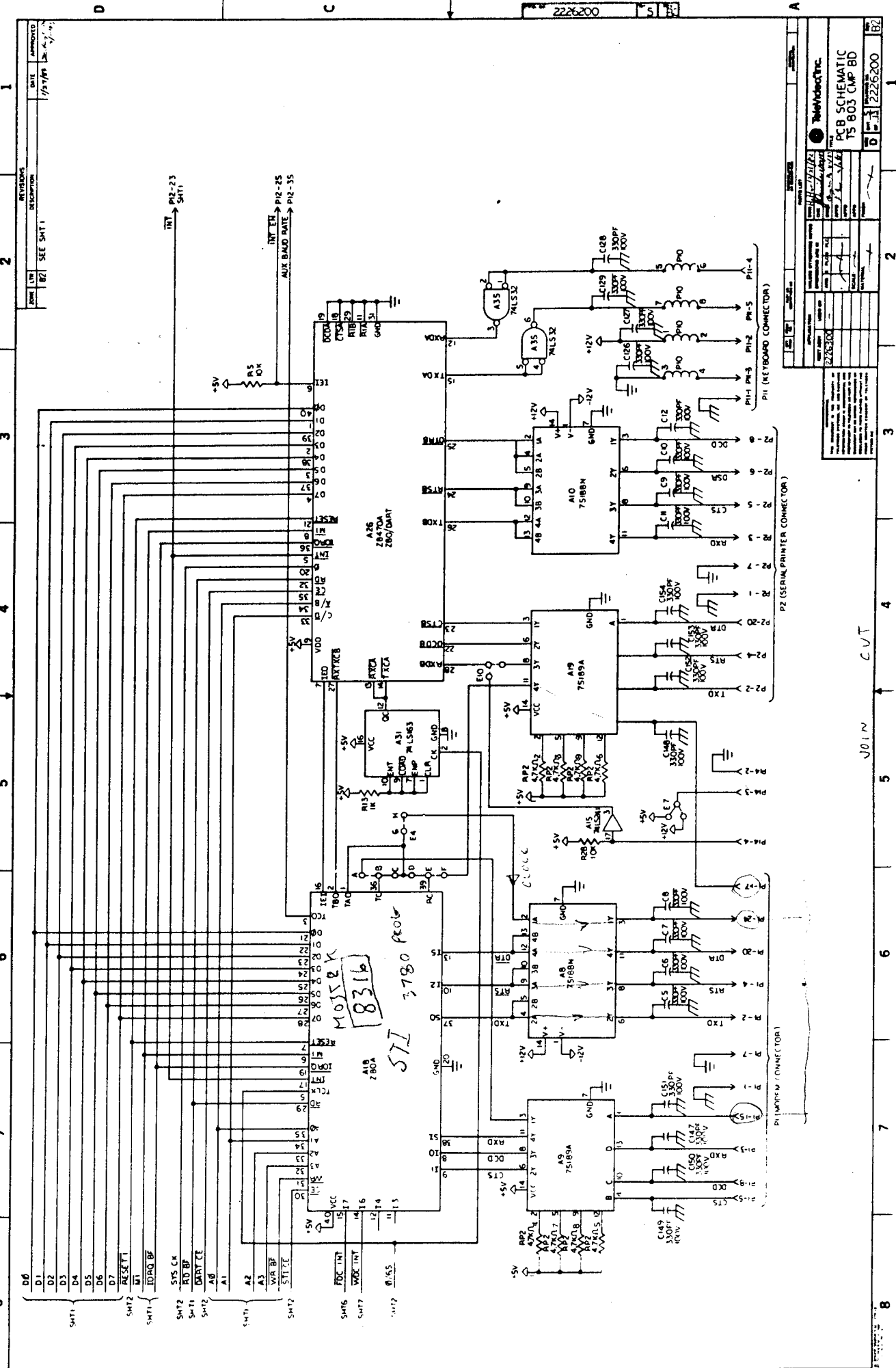
TS 803 CMP BD

2226200

2 B2



3780



REV	DATE	DESCRIPTION
1	1/5/78	SEE SMT 1

PCB SCHEMATIC	
PS 803 CMP BD	
2226200	
1	

PII (KEYBOARD CONNECTOR)	
PII-1 PII-2 PII-3 PII-4 PII-5 PII-6 PII-7 PII-8 PII-9 PII-10 PII-11 PII-12 PII-13 PII-14 PII-15 PII-16 PII-17 PII-18 PII-19 PII-20 PII-21 PII-22 PII-23 PII-24 PII-25 PII-26 PII-27 PII-28 PII-29 PII-30 PII-31 PII-32 PII-33 PII-34 PII-35 PII-36 PII-37 PII-38 PII-39 PII-40 PII-41 PII-42 PII-43 PII-44 PII-45 PII-46 PII-47 PII-48 PII-49 PII-50 PII-51 PII-52 PII-53 PII-54 PII-55 PII-56 PII-57 PII-58 PII-59 PII-60 PII-61 PII-62 PII-63 PII-64 PII-65 PII-66 PII-67 PII-68 PII-69 PII-70 PII-71 PII-72 PII-73 PII-74 PII-75 PII-76 PII-77 PII-78 PII-79 PII-80 PII-81 PII-82 PII-83 PII-84 PII-85 PII-86 PII-87 PII-88 PII-89 PII-90 PII-91 PII-92 PII-93 PII-94 PII-95 PII-96 PII-97 PII-98 PII-99 PII-100	

P2 (SERIAL PRINTER CONNECTOR)	
P2-1 P2-2 P2-3 P2-4 P2-5 P2-6 P2-7 P2-8 P2-9 P2-10 P2-11 P2-12 P2-13 P2-14 P2-15 P2-16 P2-17 P2-18 P2-19 P2-20 P2-21 P2-22 P2-23 P2-24 P2-25 P2-26 P2-27 P2-28 P2-29 P2-30 P2-31 P2-32 P2-33 P2-34 P2-35 P2-36 P2-37 P2-38 P2-39 P2-40 P2-41 P2-42 P2-43 P2-44 P2-45 P2-46 P2-47 P2-48 P2-49 P2-50 P2-51 P2-52 P2-53 P2-54 P2-55 P2-56 P2-57 P2-58 P2-59 P2-60 P2-61 P2-62 P2-63 P2-64 P2-65 P2-66 P2-67 P2-68 P2-69 P2-70 P2-71 P2-72 P2-73 P2-74 P2-75 P2-76 P2-77 P2-78 P2-79 P2-80 P2-81 P2-82 P2-83 P2-84 P2-85 P2-86 P2-87 P2-88 P2-89 P2-90 P2-91 P2-92 P2-93 P2-94 P2-95 P2-96 P2-97 P2-98 P2-99 P2-100	

PI (PRINTER CONNECTOR)	
PI-1 PI-2 PI-3 PI-4 PI-5 PI-6 PI-7 PI-8 PI-9 PI-10 PI-11 PI-12 PI-13 PI-14 PI-15 PI-16 PI-17 PI-18 PI-19 PI-20 PI-21 PI-22 PI-23 PI-24 PI-25 PI-26 PI-27 PI-28 PI-29 PI-30 PI-31 PI-32 PI-33 PI-34 PI-35 PI-36 PI-37 PI-38 PI-39 PI-40 PI-41 PI-42 PI-43 PI-44 PI-45 PI-46 PI-47 PI-48 PI-49 PI-50 PI-51 PI-52 PI-53 PI-54 PI-55 PI-56 PI-57 PI-58 PI-59 PI-60 PI-61 PI-62 PI-63 PI-64 PI-65 PI-66 PI-67 PI-68 PI-69 PI-70 PI-71 PI-72 PI-73 PI-74 PI-75 PI-76 PI-77 PI-78 PI-79 PI-80 PI-81 PI-82 PI-83 PI-84 PI-85 PI-86 PI-87 PI-88 PI-89 PI-90 PI-91 PI-92 PI-93 PI-94 PI-95 PI-96 PI-97 PI-98 PI-99 PI-100	

PII (KEYBOARD CONNECTOR)	
PII-1 PII-2 PII-3 PII-4 PII-5 PII-6 PII-7 PII-8 PII-9 PII-10 PII-11 PII-12 PII-13 PII-14 PII-15 PII-16 PII-17 PII-18 PII-19 PII-20 PII-21 PII-22 PII-23 PII-24 PII-25 PII-26 PII-27 PII-28 PII-29 PII-30 PII-31 PII-32 PII-33 PII-34 PII-35 PII-36 PII-37 PII-38 PII-39 PII-40 PII-41 PII-42 PII-43 PII-44 PII-45 PII-46 PII-47 PII-48 PII-49 PII-50 PII-51 PII-52 PII-53 PII-54 PII-55 PII-56 PII-57 PII-58 PII-59 PII-60 PII-61 PII-62 PII-63 PII-64 PII-65 PII-66 PII-67 PII-68 PII-69 PII-70 PII-71 PII-72 PII-73 PII-74 PII-75 PII-76 PII-77 PII-78 PII-79 PII-80 PII-81 PII-82 PII-83 PII-84 PII-85 PII-86 PII-87 PII-88 PII-89 PII-90 PII-91 PII-92 PII-93 PII-94 PII-95 PII-96 PII-97 PII-98 PII-99 PII-100	

REV	DATE	DESCRIPTION
1	1/15/83	SEE SH11

2226200	6	2
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PCB SCHEMATIC	TS B03 CMP B0
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2226200	6	2
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PCB SCHEMATIC	TS B03 CMP B0
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2226200	6	2
---------	---	---

PCB SCHEMATIC	TS B03 CMP B0
---------------	---------------

2226200	6	2
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PCB SCHEMATIC	TS B03 CMP B0
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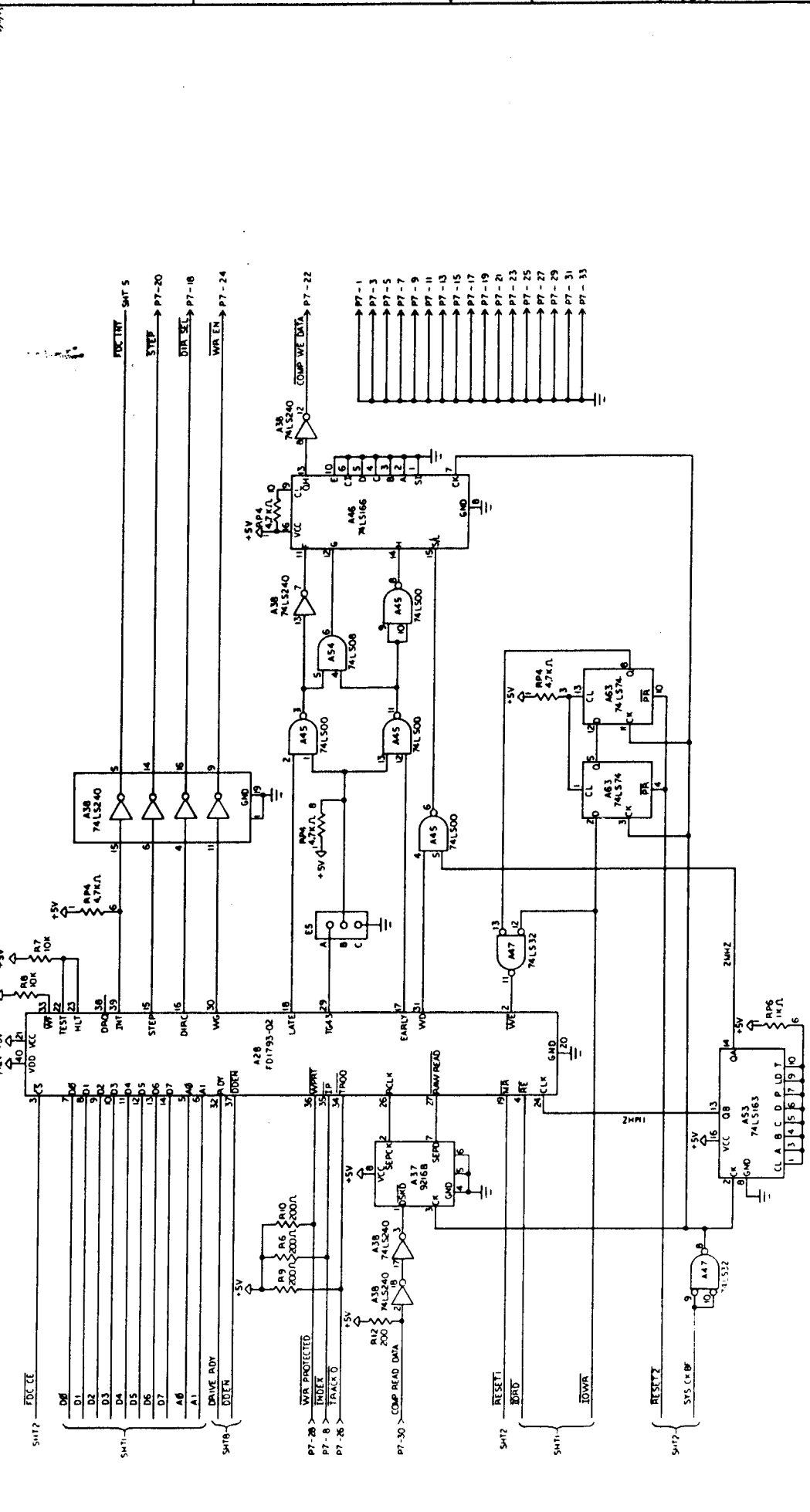
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PCB SCHEMATIC	TS B03 CMP B0
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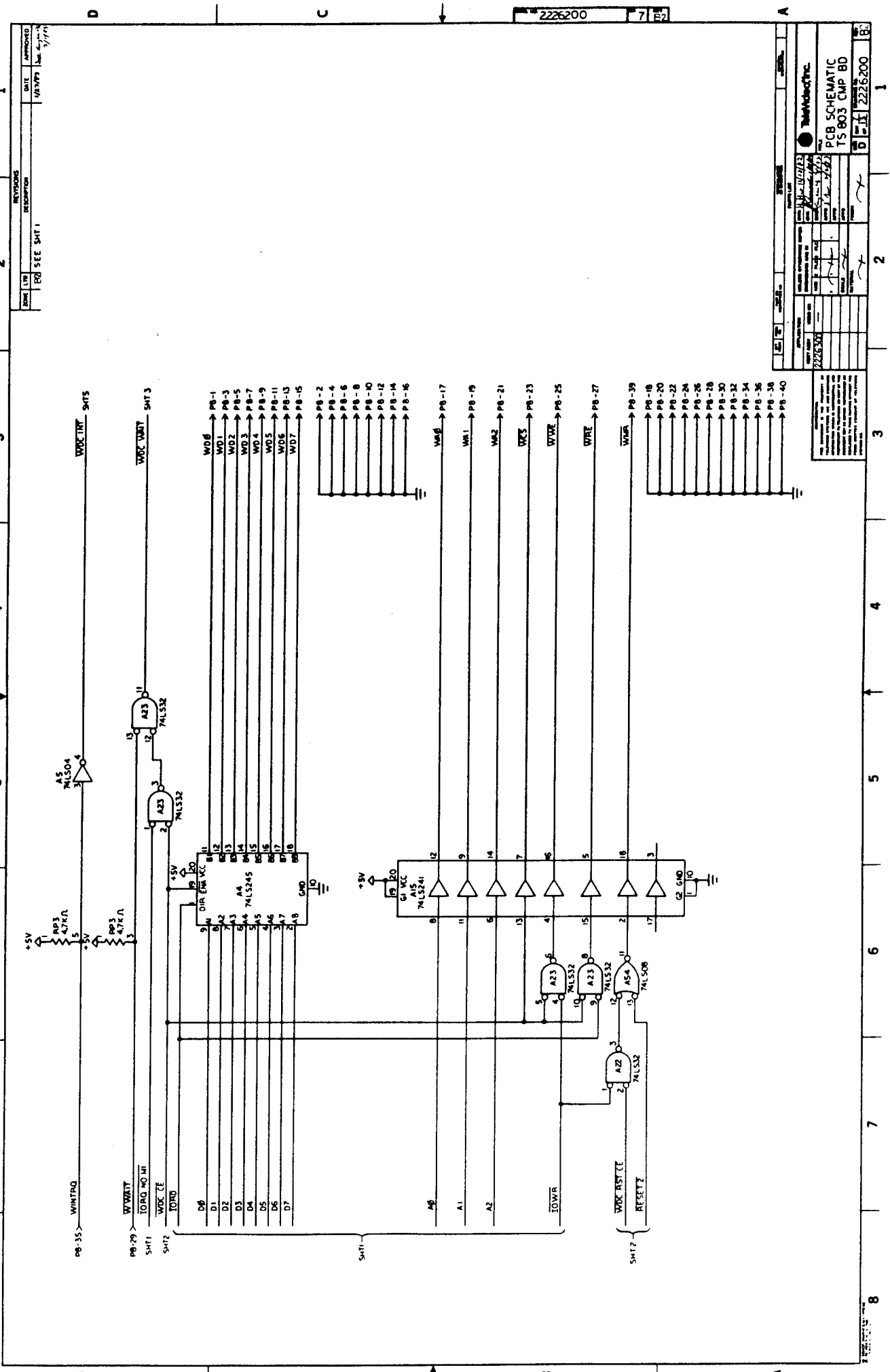
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PCB SCHEMATIC	TS B03 CMP B0
---------------	---------------

2226200	6	2
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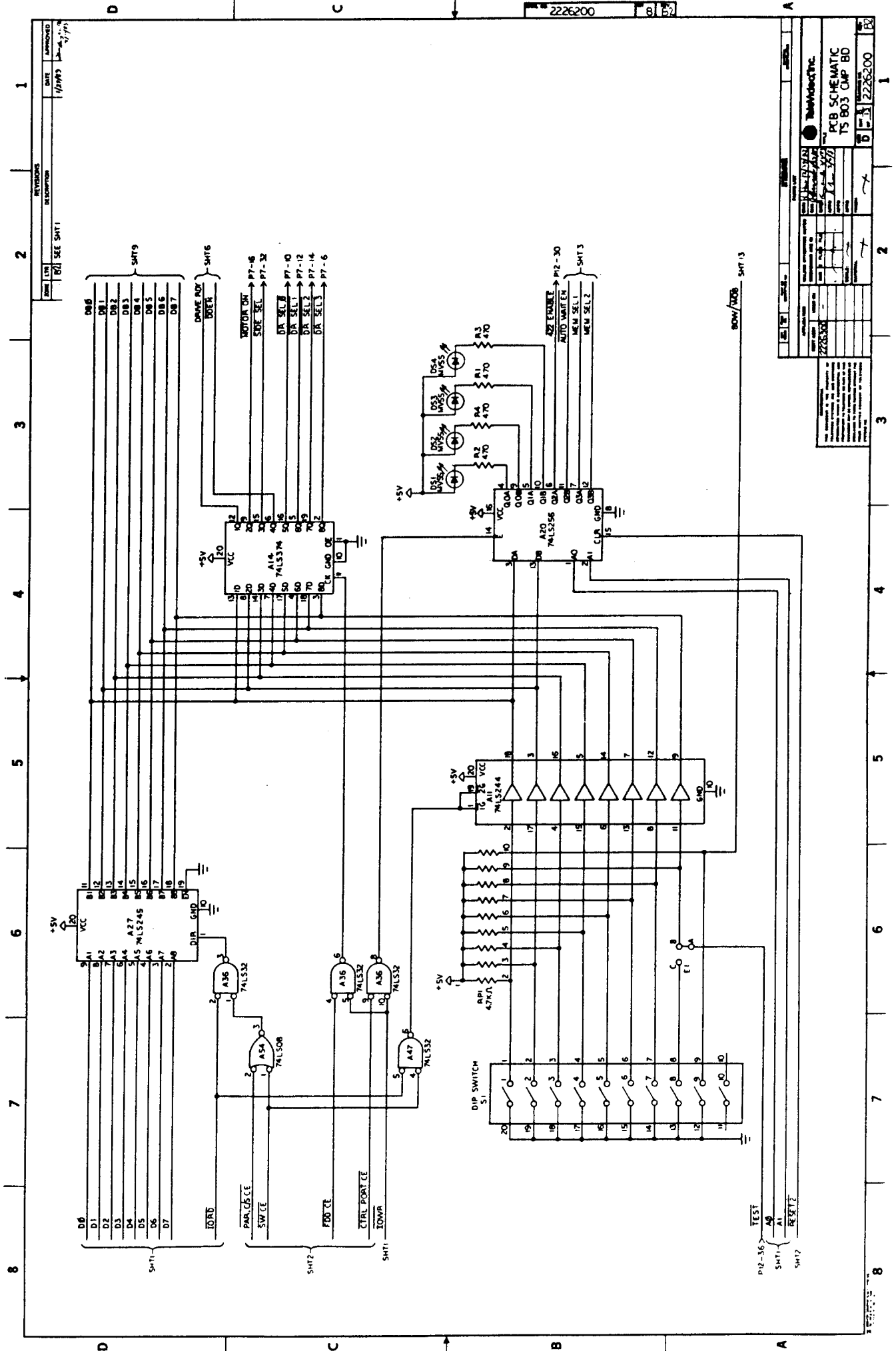
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REV	DATE	DESCRIPTION
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2226200	7	B2
PCB SCHEMATIC		
TS 803 CUP BD		
2226200		

TS 803 CUP BD
2226200



REV	DATE	DESCRIPTION
1	11/1/83	DO SEE SMT 1

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

PCB SCHEMATIC
TS 803 CMP BD

2226200

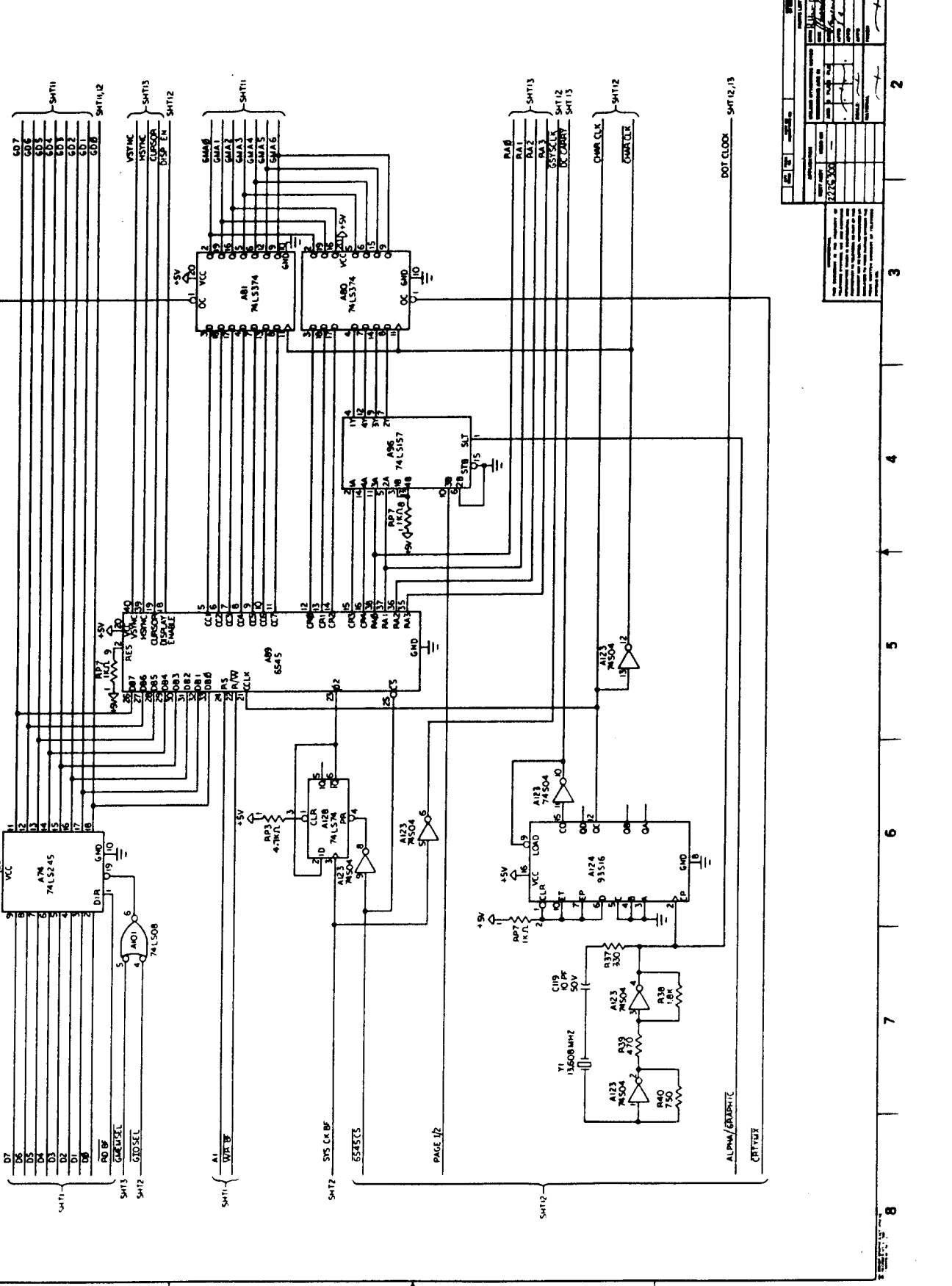
PCB SCHEMATIC
TS 803 CMP BD

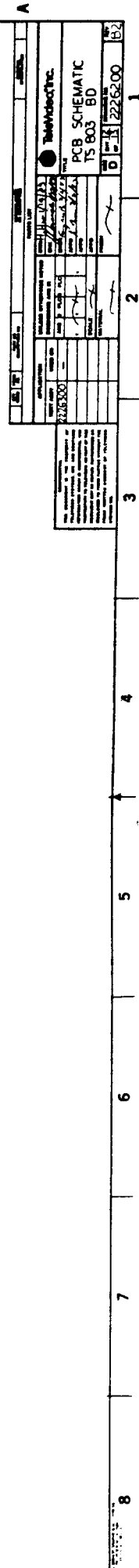
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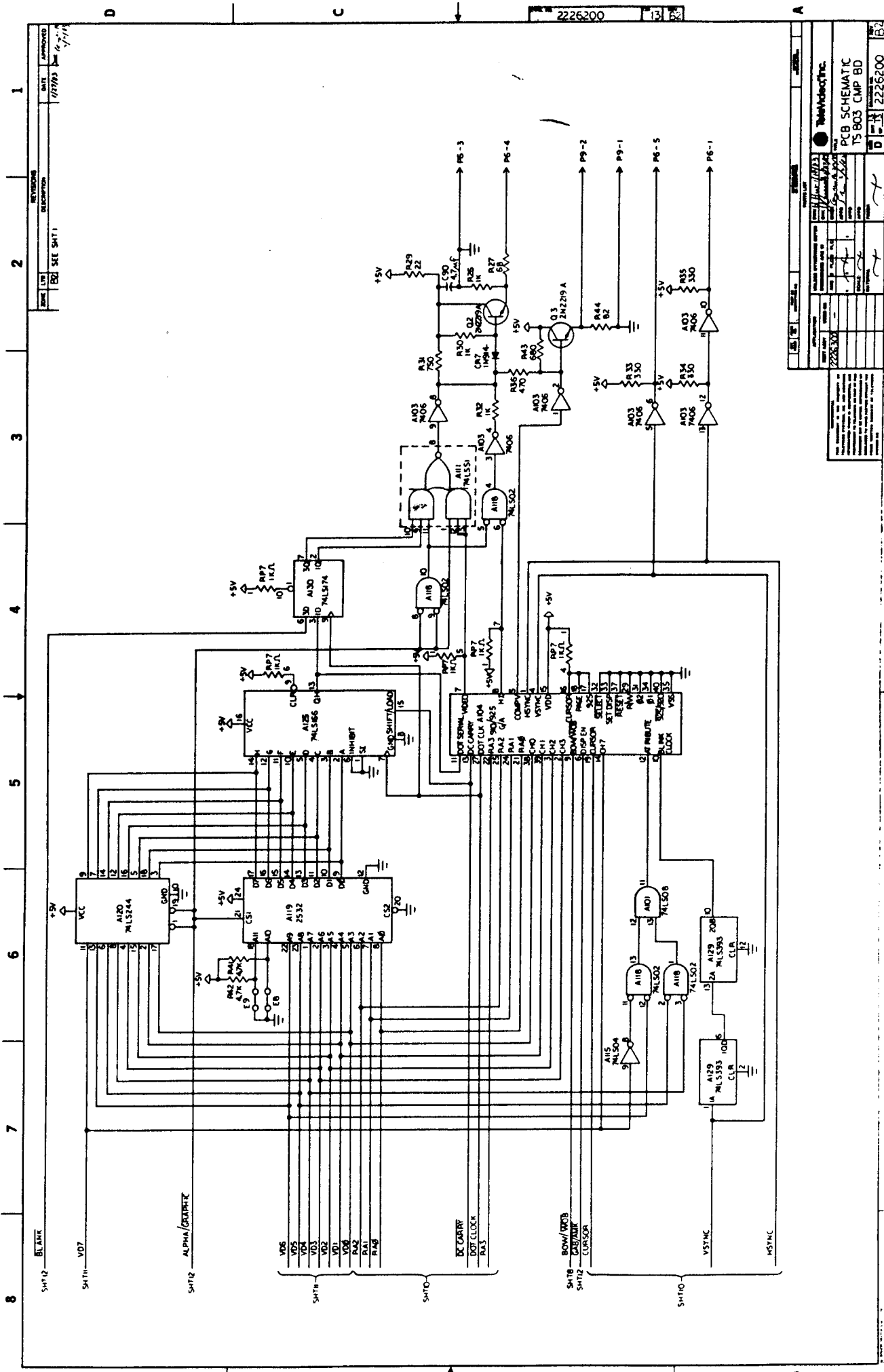
PCB SCHEMATIC
TS 803 CMP BD

2226200

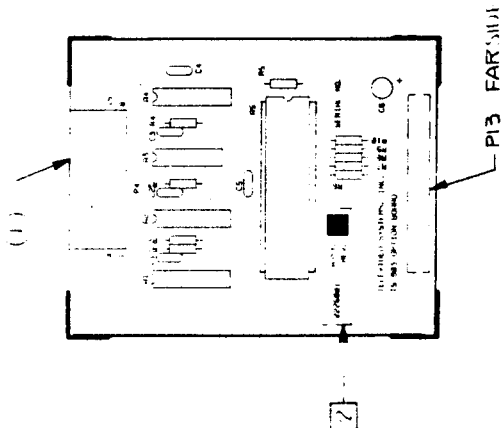
PCB SCHEMATIC
TS 803 CMP BD





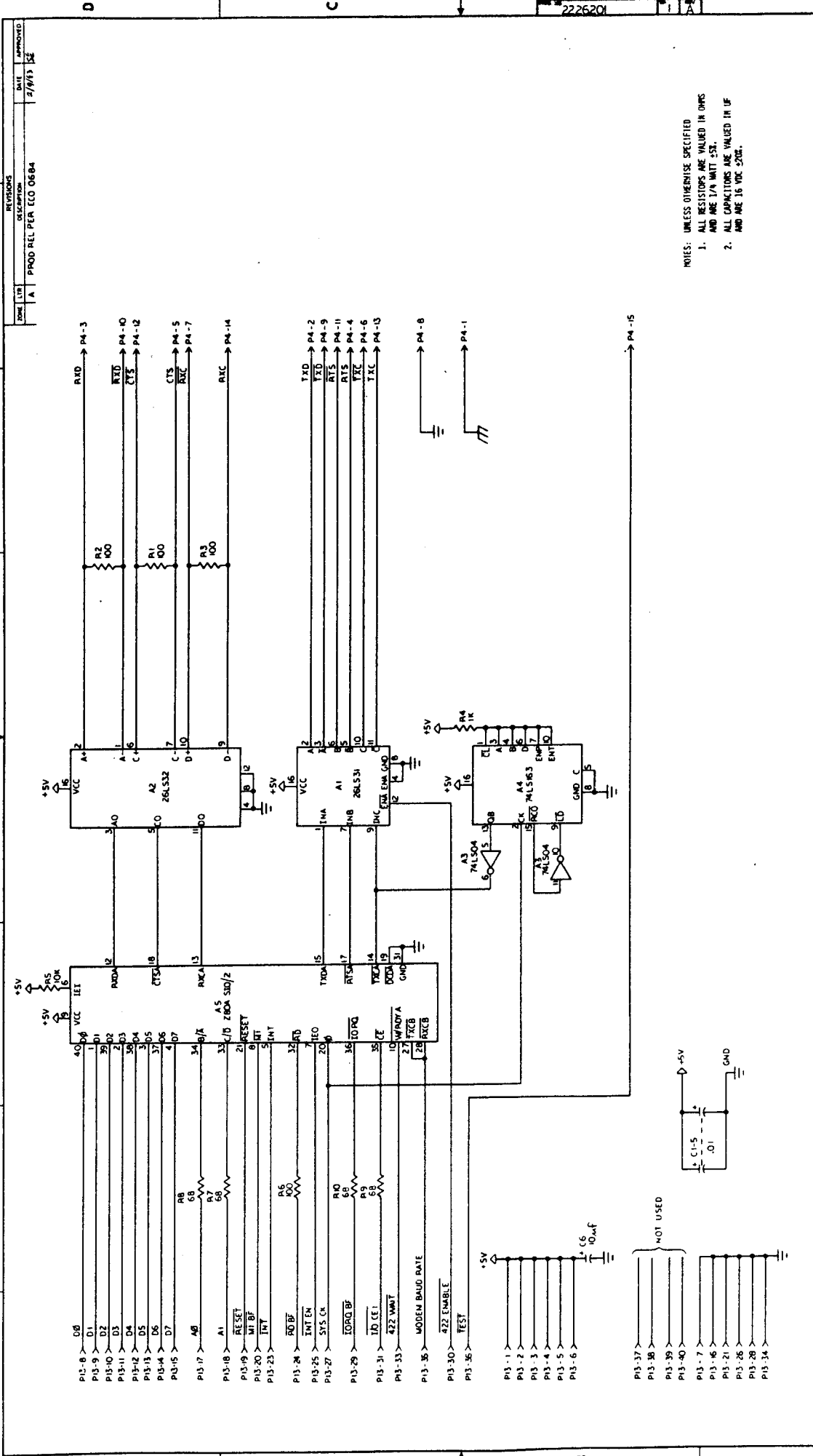


APPLICATION	REVISION	DATE	BY
ASSY	A	10/10/74	REL
25100			



- NOTE: UNLESS OTHERWISE SPECIFIED
1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
 2. SILKSCREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK 50-100X APPROXIMATELY WHERE SHOWN.
 3. MADE FROM 2226101 FAB REV A.

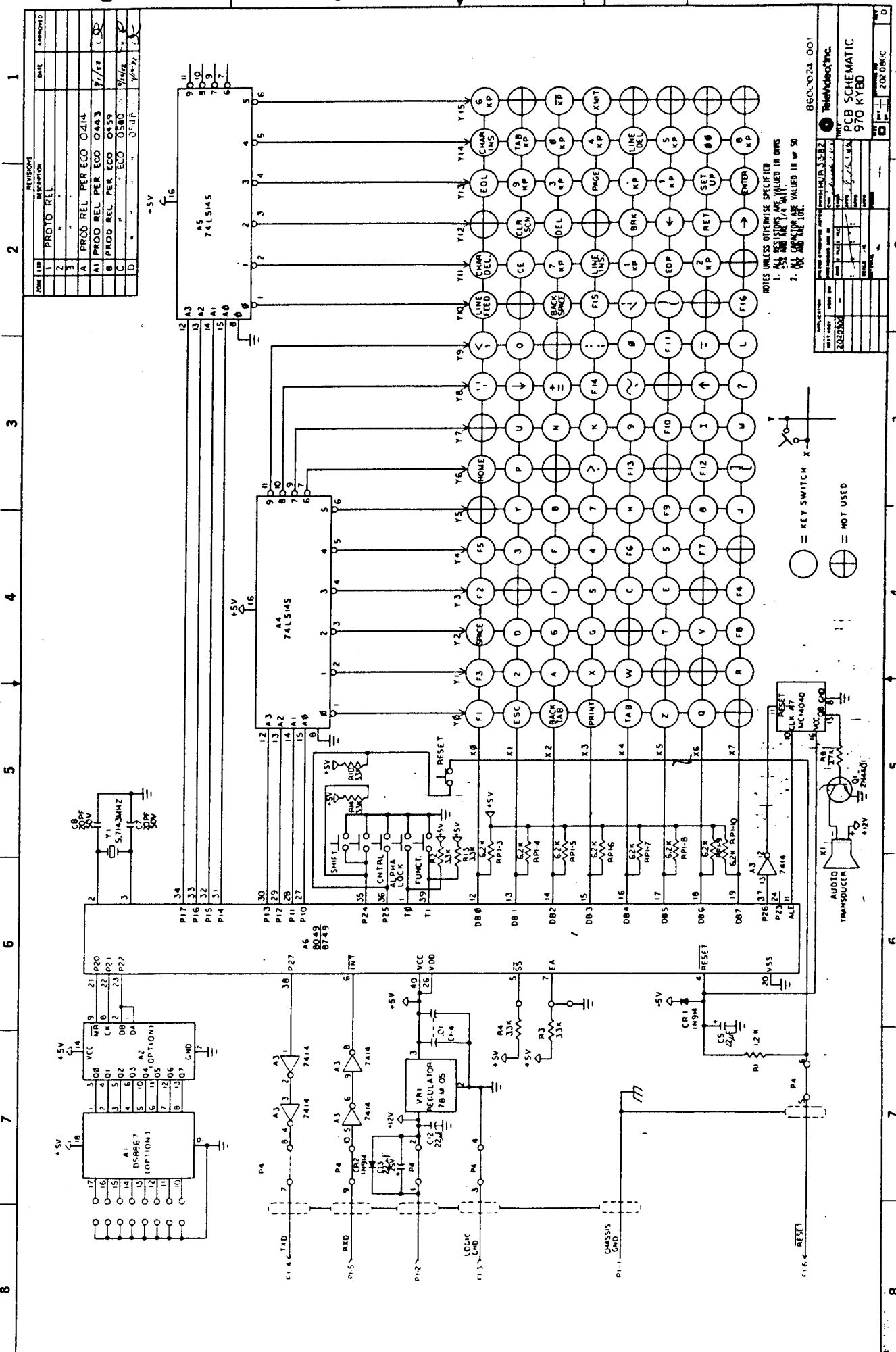
IceVideo Systems, Inc. 10B ASSY DWG 10 803 OPT CMP BD		SHEET 1 OF 1 SUPERSEDES
MATERIAL DIMENSION 2.00 INCH AREA 4.00 INCH	TOLERANCES UNLESS NOTED DIMENSION 2.00 INCH AREA 4.00 INCH	DATE 10/10/74 DATE 10/10/74 CUSTOMER APPROVAL
CONFIDENTIAL THIS DOCUMENT IS THE PROPERTY OF ICEVIDEO SYSTEMS, INC. AND CONTAINS INFORMATION THAT IS UNCLASSIFIED AND UNCONTROLLED. IT IS TO BE RETURNED TO THE ORIGINATOR IF IT IS DISCOVERED BY AN UNAUTHORIZED PERSON. IT IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.		SIZE C CODE IDENT 2226301 REV A



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE VALUED IN OHMS
 AND ARE 1/4 WATT 5%.
 2. ALL CAPACITORS ARE VALUED IN UF
 AND ARE 16 VDC 50%.

REVISIONS		DATE	APPROVED
1	PROD REL PER ECO 0684	2/8/13	
2226201 PCB SCHEMATIC 15803 OPT CMP BD 2226201			

ZONE	LTP	REVISIONS		DATE	APPROVED
		DESCRIPTION			
1		PROTO REL			
2		"			
3		"			
A		PROD REL PER ECO 0214			
B		PROD REL PER ECO 0443		7/1/52	CR
C		PROD REL PER ECO 0459			
D		" " ECO 0580		9/1/52	CR
E		" " ECO 0580		9/1/52	CR

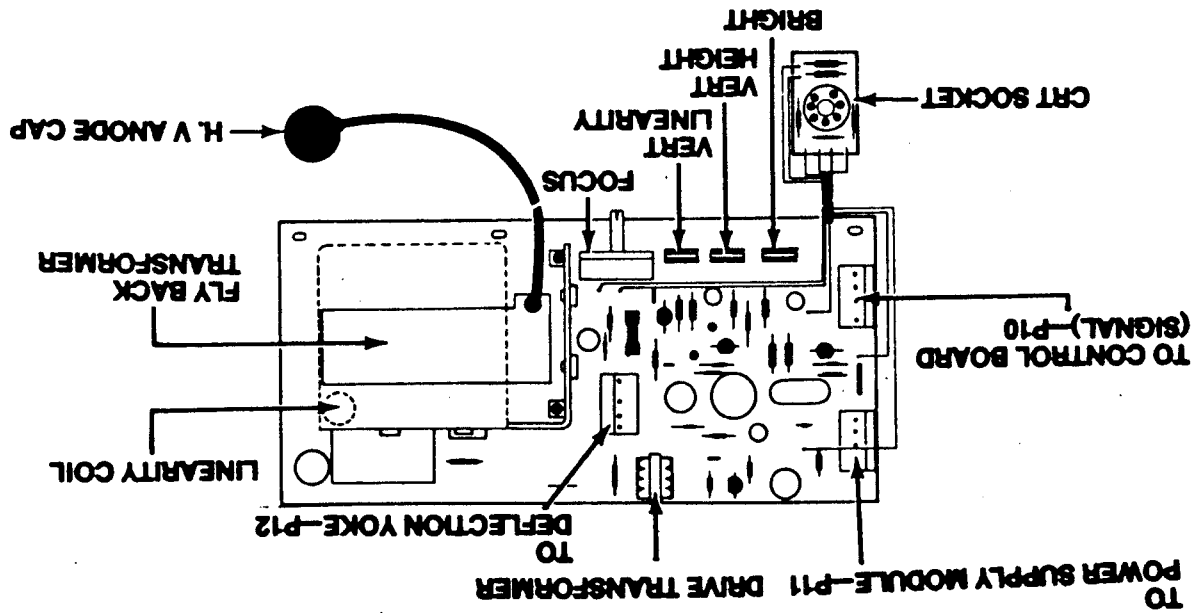


NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS
5% AND ARE 1/4 WATT.
2. ALL CAPACITORS ARE VALUED IN μ F 50
VOLT AND 10% TOL.

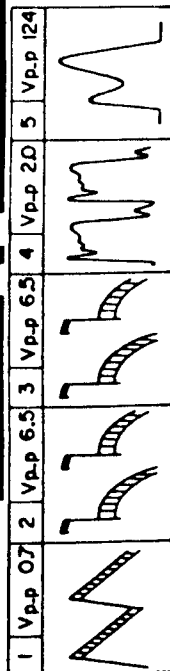
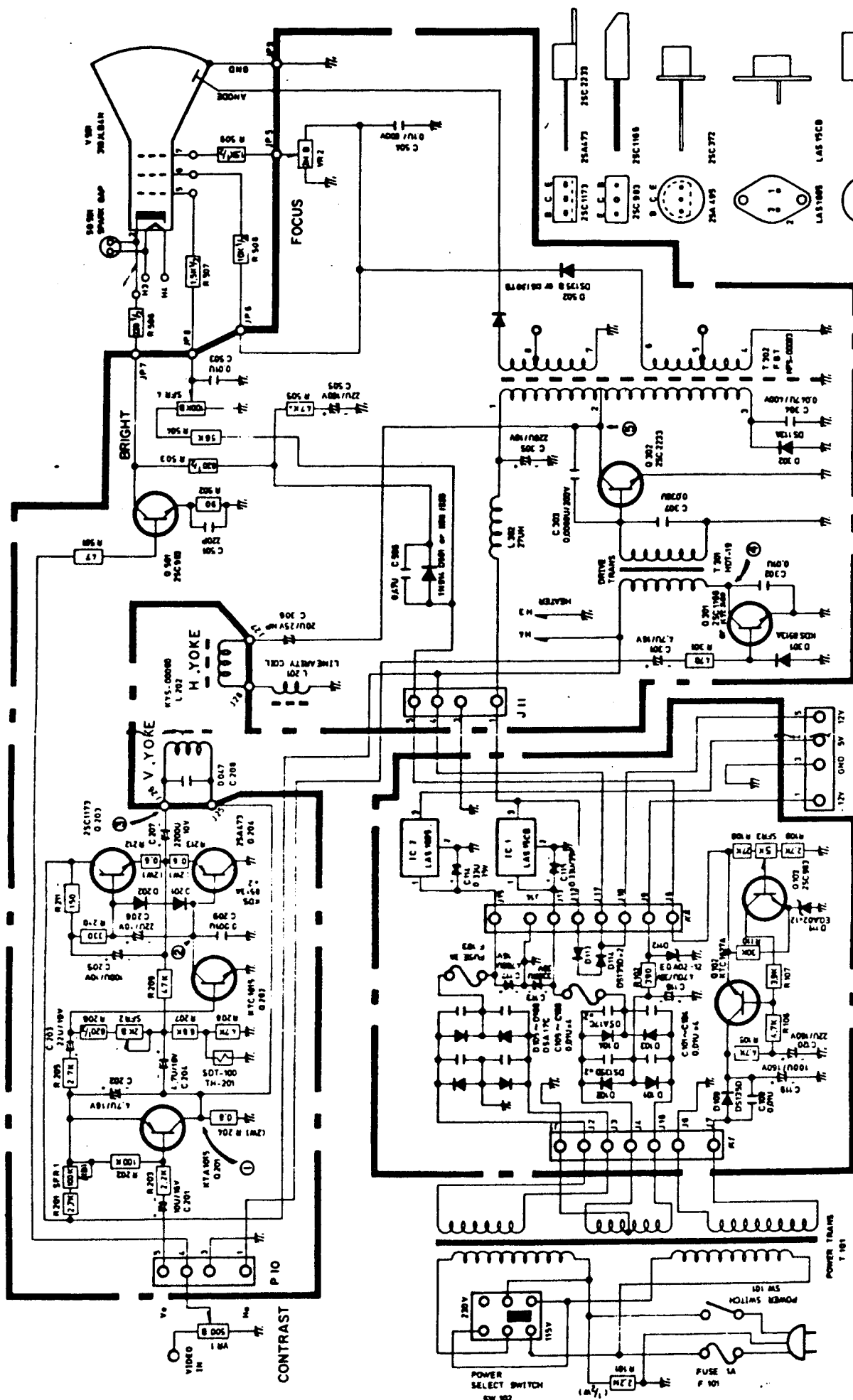
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Location of Components on Video Module



V - HEIGHT

V - LINEARITY

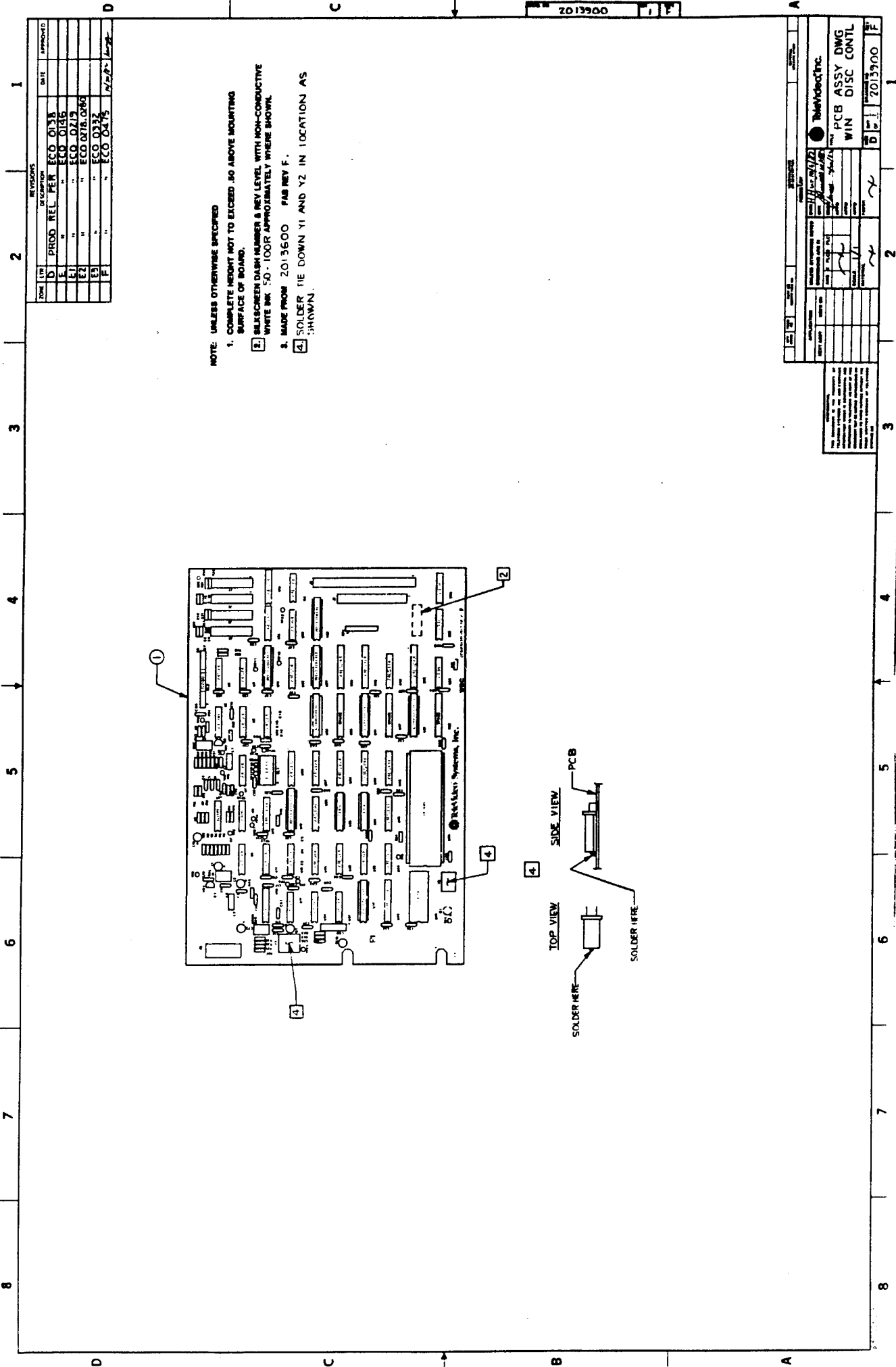


1. All resistance values in OHM K=1,000 M=1,000,000.

2. All capacitor values in FARAD U=10⁶ P=10¹².

3. Unless otherwise stated, working voltages of capacitors are 50 volts.

4. This schematic diagram covers basic or representative chassis only. There may be some component or partial schematic difference between actual chassis and the schematic diagram.



REVISIONS			DATE	APPROVED
1	PROG REL PER	ECO 0138		
2	"	ECO 0146		
3	"	ECO 0219		
4	"	ECO 0219		
5	"	ECO 0219		
6	"	ECO 0219		
7	"	ECO 0219		
8	"	ECO 0219		
9	"	ECO 0219		
10	"	ECO 0219		
11	"	ECO 0219		
12	"	ECO 0219		
13	"	ECO 0219		
14	"	ECO 0219		
15	"	ECO 0219		
16	"	ECO 0219		
17	"	ECO 0219		
18	"	ECO 0219		
19	"	ECO 0219		
20	"	ECO 0219		

- NOTE: UNLESS OTHERWISE SPECIFIED
1. COMPLETE HEIGHT NOT TO EXCEED .50 ABOVE MOUNTING SURFACE OF BOARD.
 2. SILKSCHREEN DASH NUMBER & REV LEVEL WITH NON-CONDUCTIVE WHITE INK .50 - .100R APPROXIMATELY WHERE SHOWN.
 3. MADE FROM 2013600 PAB REV F.
 4. SOLDER IE DOWN Y1 AND Y2 IN LOCATION AS SHOWN.

REVISIONS			DATE	APPROVED
1	PROG REL PER	ECO 0138		
2	"	ECO 0146		
3	"	ECO 0219		
4	"	ECO 0219		
5	"	ECO 0219		
6	"	ECO 0219		
7	"	ECO 0219		
8	"	ECO 0219		
9	"	ECO 0219		
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11	"	ECO 0219		
12	"	ECO 0219		
13	"	ECO 0219		
14	"	ECO 0219		
15	"	ECO 0219		
16	"	ECO 0219		
17	"	ECO 0219		
18	"	ECO 0219		
19	"	ECO 0219		
20	"	ECO 0219		

PCB ASSY DWG
WIN DISC CONTL

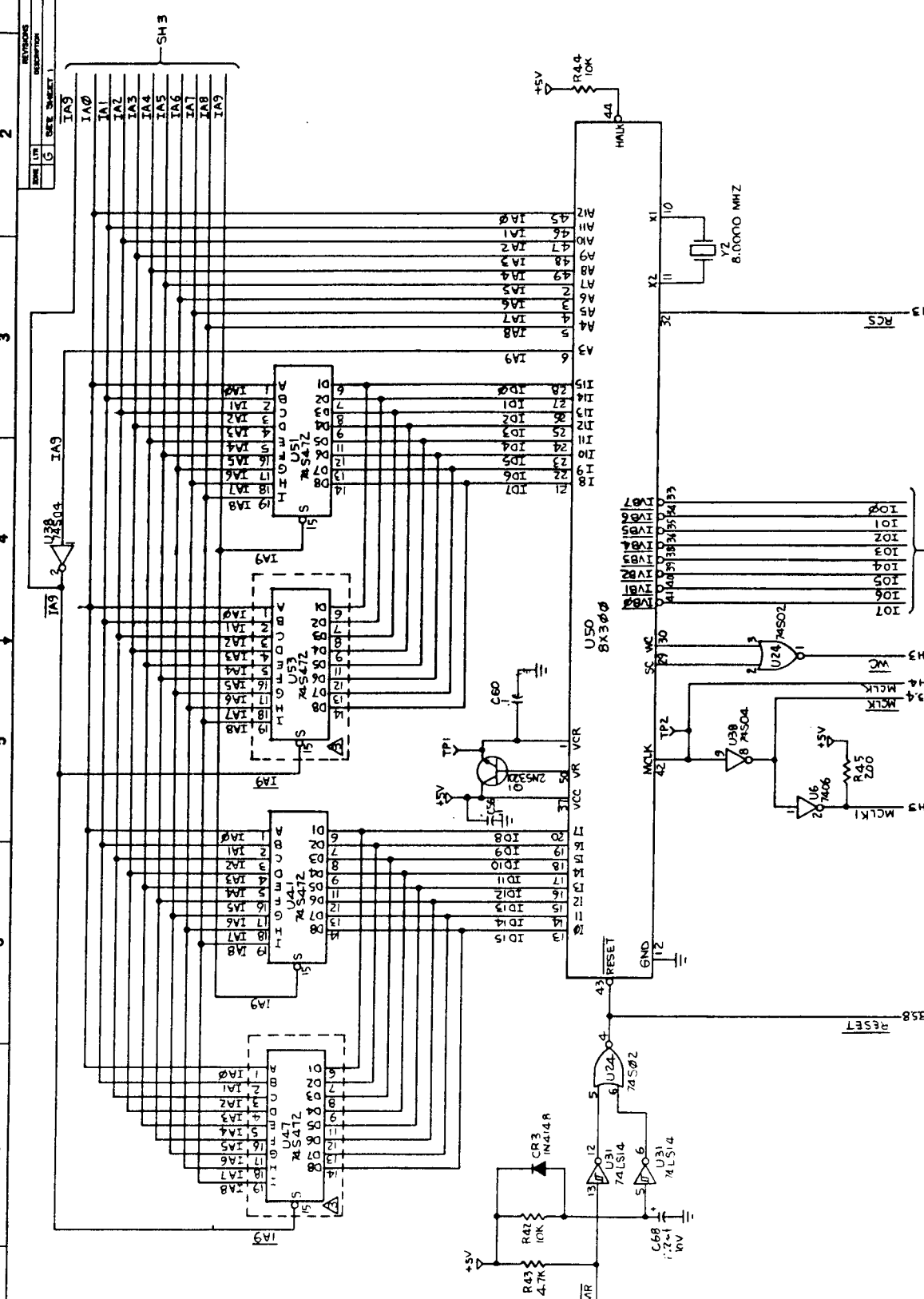
8	7	6	5	4	3	2	1
MEMORIC		MEANING		MEANING		REVISIONS	
ANDT	ADDRESS MARK DETECT	-SEEK COMPLETE SEARCH	SEEK COMPLETE STATUS FROM DRIVE	DATE	DESCRIPTION	DATE	APPROVED
A2-A0	TASK FILE ADDRESS SELECT BITS 2-0	-STEP PULSE	STEP PULSE TO DRIVE	4/2/74	ECO 0725	4/2/74	ALS
BIC	BUS INPUT CONTROL	TIMCLK	TIMING CLOCK FOR SAI000		ECO 0725		
BOC	BUS OUTPUT CONTROL	TRACK 000	TRACK 000 STATUS FROM DRIVE		ECO 0725		
CLKS	CLOCK DATA	WAEEN	WAIT ENABLE		ECO 0725		
CRCIZ	CYCLIC REDUNDANCY CHECK WORD INITIALIZE	WAIT	MEMORY NOT READY SIGNAL		ECO 0725		
CRCLK	CRC OKAY	WCLK	WRITE CLOCK		ECO 0725		
CS	CARD SELECT	WE	WRITE ENABLE		ECO 0725		
CSAC	CARD SELECT ACCESS CONTROL	WGI	WRITE GATE INTERNAL		ECO 0725		
DAL7-DAL0	DATA ACCESS LINE	-WRITE FAULT	WRITE FAULT STATUS FROM DRIVE		ECO 0725		
-DIRECTION IN	DIRECTION CONTROL	WR7-WR0	WRITE CONTROL LINES		ECO 0725		
DHOLD	DATA HOLD	IBLA	1 BYTE LOOK AHEAD		ECO 0725		
DLYDAT	DELAYED DATA	ZADR	2 X DATA REFERENCE CLOCK		ECO 0725		
DRQ	DATA REQUEST						
DRQCLK	DATA REQUEST CLOCK						
DRSEL	DRIVE SELECT						
DRS4-DRS1	DRIVE SELECT BITS 4-1						
DRUN	DATA RUN						
HFREQ	HIGH FREQUENCY						
HSAC	HOST SELECT ACCESS CONTROL						
HS2-HS0	HEAD SELECT BITS 2-0						
IA9-IA0	INSTRUCTION ADDRESS LINES BITS 9-0						
IDIS-ID0	INSTRUCTION DATA BITS 15-0						
INDEX	INDEX PULSE FROM DRIVE						
INTCLK	INTERRUPT CLOCK						
INTRQ	INTERRUPT REQUEST						
I07-I00	I/O LINES 7-0						
IVB0-IVR7	INPUT VECTOR BUS BITS 0-7						
MCLK	MASTER CLOCK						
MFMAW	MODIFIED FREQUENCY MODULATION WRITE STREAM						
MR	MASTER RESET						
OSC	OSCILLATOR OUTPUT						
RA9-RA0	RAM ADDRESS BITS 9-0						
RCLK	READ CLOCK						
RCS	RAM CHIP SELECT						
RDAT	READ DATA						
RD6-RD4 RD2 RD0	READ CONTROL LINES						
RE	READ ENABLE						
-READY	READY STATUS FROM DRIVE						
RESET	RESET SIGNAL						
RGATE	READ GATE						
ROV	RAM OVERFLOW						
1-WC	REDUCE WRITE CURRENT						
NOTE: UNLESS OTHERWISE SPECIFIED		1. RESISTOR VALUES ARE IN OHMS $\pm 5\%$, $1/4$ W		2. JUMPER E5 TO E4 TO QUALIFY WAIT BY CS		3. JUMPER E3 TO E4 IF BIT-BOC TO QUALIFY WAIT	
		4. ALL CAPACITOR ARE VALUED IN μ F 50V AND ARE 10%		5. NOT USED ONLY WHEN FOR EXPANDING		6. MEMORY TO IK.	
		7. NOT USED FOR 5 1/4" DRIVE.		8. J7 IS FOR 5 1/4" DRIVE. J0 IS FOR 8" DRIVE.			

NOTES: VALUES OTHERWISE SPECIFIED

- RESISTOR VALUES ARE IN OHMS $\pm 5\%$, $\frac{1}{4}$ W.
- JUMPER E5 TO E4 TO QUALIFY WAIT BY CS
- JUMPER E3 TO E4 IF BIC-BOC TO QUALIFY WAIT
- NOT USED, USED ONLY WHEN FOR EXPANDING MEMORY TO 1K.
- ALL CAPACITOR ARE VALUED IN μ F 50V AND ARE 10%.
- NOT USED FOR $\frac{5}{16}$ " DRIVE.
- J7 IS FOR 5 $\frac{1}{4}$ " DRIVE. J0 IS FOR 8" DRIVE.

2013800

REV	DATE	BY	CHKD	APP'D
1	10/1/80	J. H. H.	J. H. H.	J. H. H.
PCB SCHEMATIC				
WIN DISC CONT				
2013800				
2013800				
2013800				

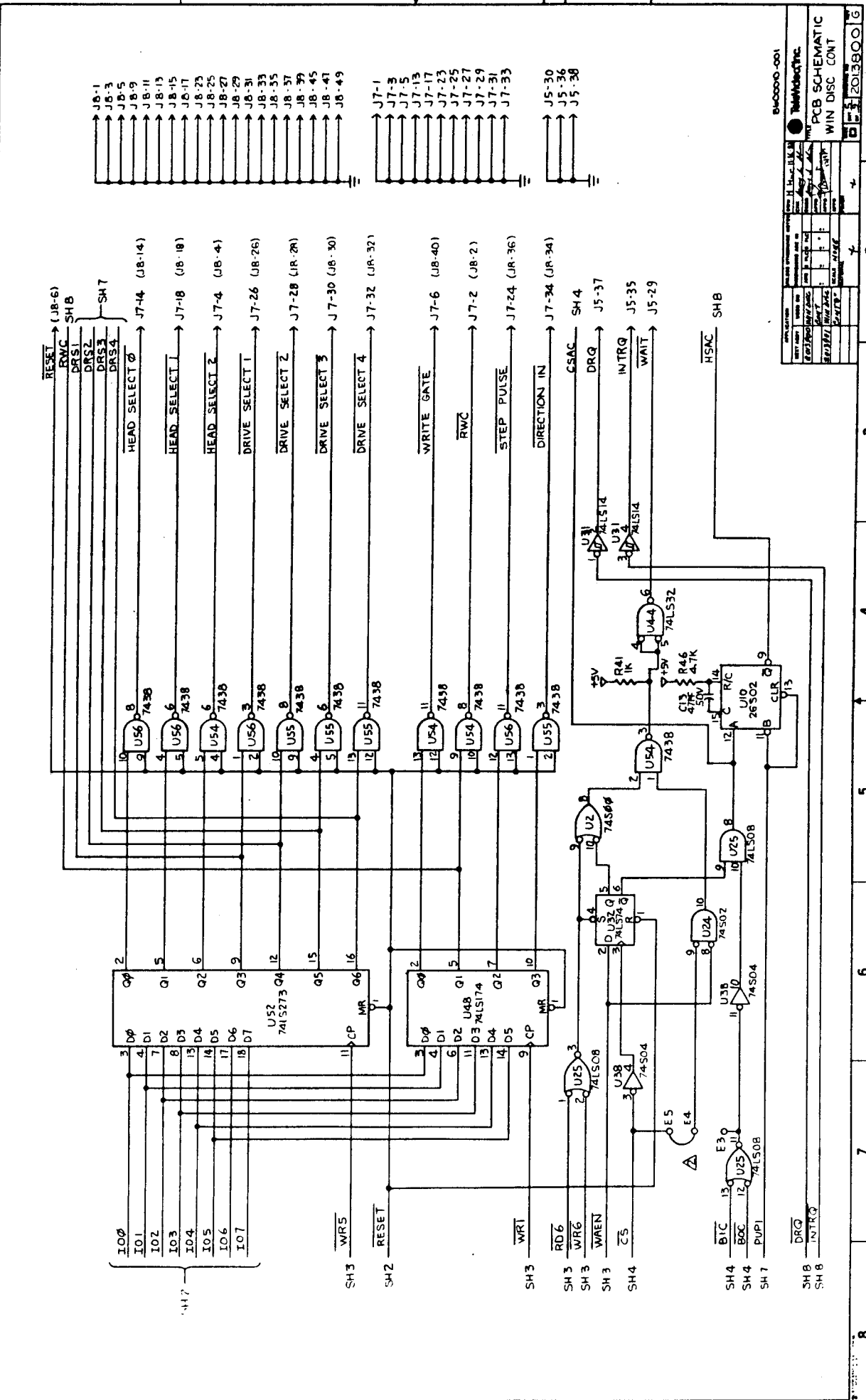


REV	DATE	DESCRIPTION	APPROVED
1	05/01/80	PCB SCHEMATIC	
2	05/01/80	WIN DISC CONT	
3	05/01/80	PCB SCHEMATIC	
4	05/01/80	WIN DISC CONT	
5	05/01/80	PCB SCHEMATIC	
6	05/01/80	WIN DISC CONT	
7	05/01/80	PCB SCHEMATIC	
8	05/01/80	WIN DISC CONT	

REV	DATE	APPROVED
1		
2		
3		
4		
5		
6		
7		
8		

REV	DATE	APPROVED
1		
2		
3		
4		
5		
6		
7		
8		

2013800



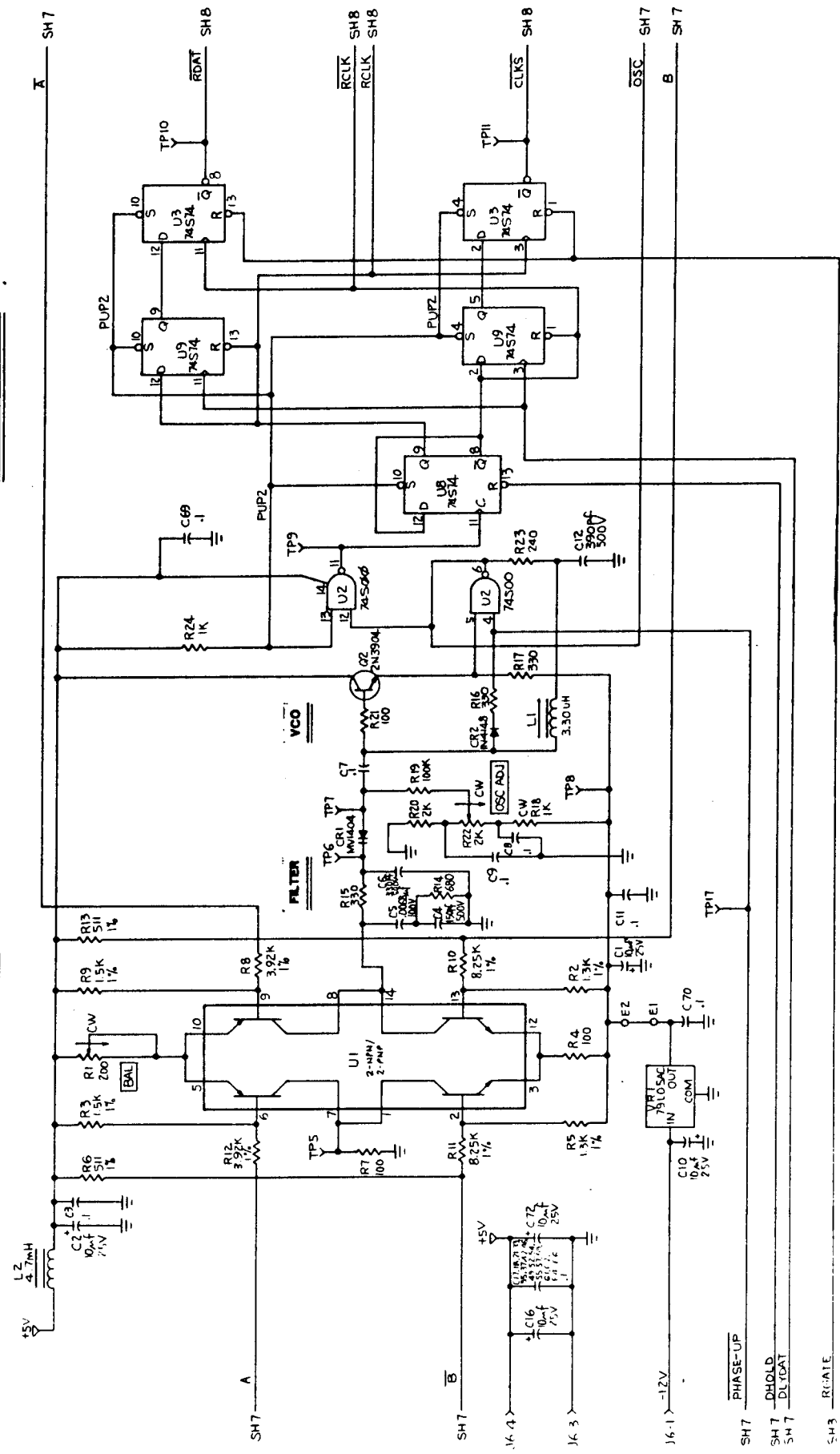
REV	DATE	APPROVED
1		
2		
3		
4		
5		
6		
7		
8		

2013800

DATE	REV	DESCRIPTION	DATE	APPROVED
	G	SEE SHEET 1		

DATA/CLOCK SEPARATOR

ERROR AMPLIFIER

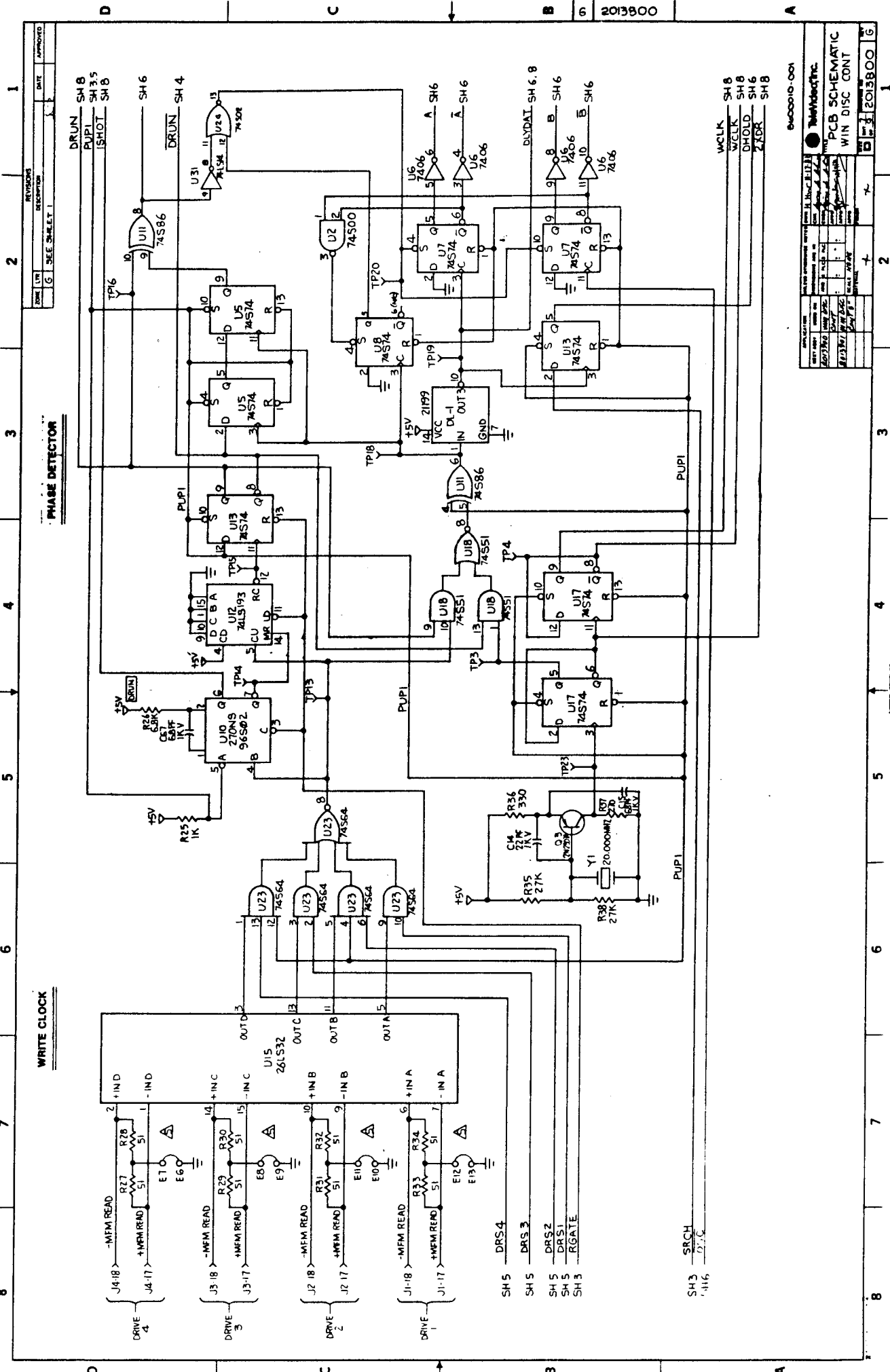


2013800-001

DATE	REV	DESCRIPTION	DATE	APPROVED
	G	SEE SHEET 1		

DATE	REV	DESCRIPTION	DATE	APPROVED
	G	SEE SHEET 1		

2013800-001



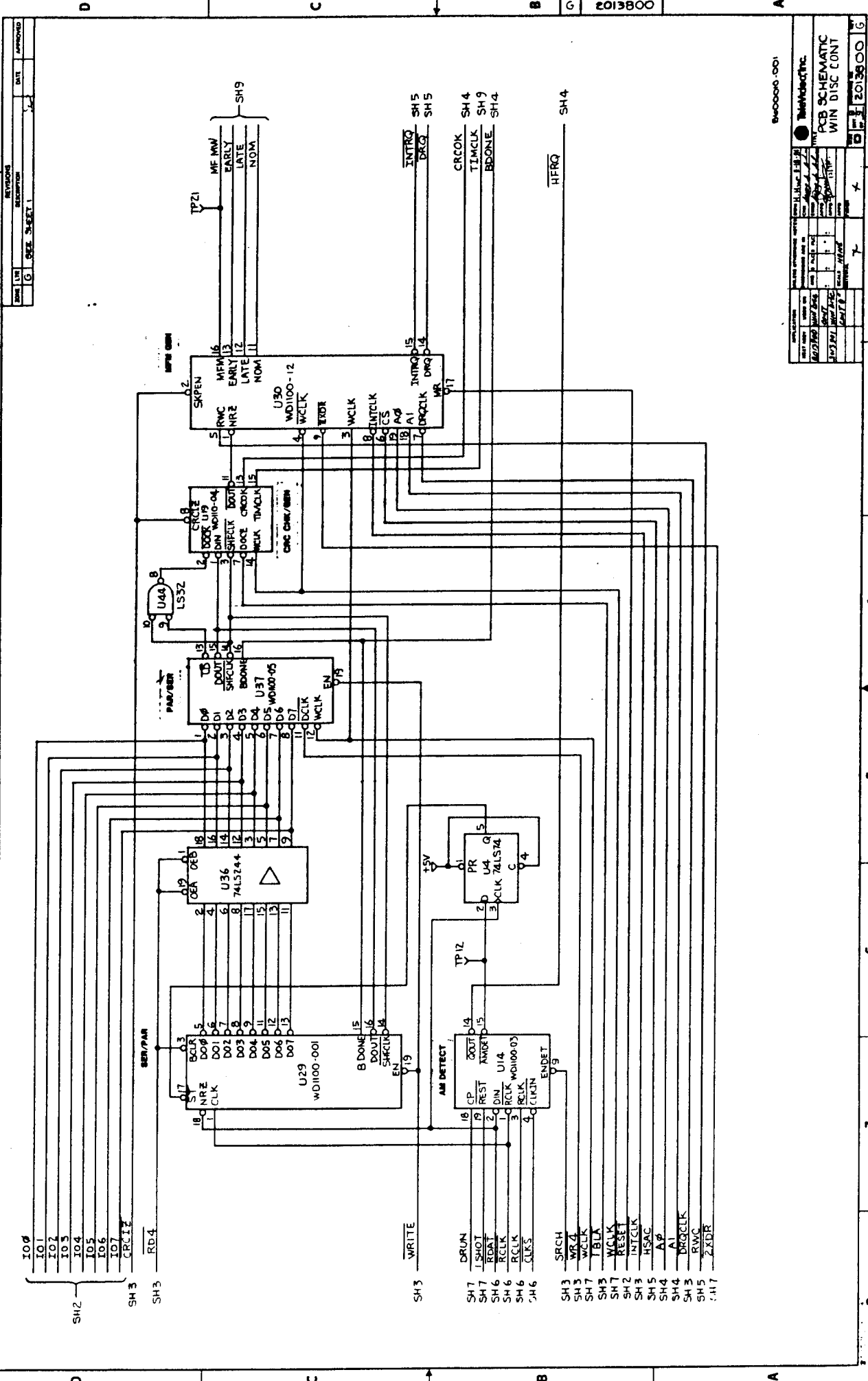
PHASE DETECTOR

WRITE CLOCK

DATE	REV	DESCRIPTION	DATE	REV	DESCRIPTION
10/1/80	1	PCB SCHEMATIC	10/1/80	1	PCB SCHEMATIC
10/1/80	2	WIN DISC CONT	10/1/80	2	WIN DISC CONT
10/1/80	3	2013800	10/1/80	3	2013800
10/1/80	4	2013800	10/1/80	4	2013800
10/1/80	5	2013800	10/1/80	5	2013800
10/1/80	6	2013800	10/1/80	6	2013800
10/1/80	7	2013800	10/1/80	7	2013800
10/1/80	8	2013800	10/1/80	8	2013800

DATE	REV	DESCRIPTION	DATE	REV	DESCRIPTION
10/1/80	1	PCB SCHEMATIC	10/1/80	1	PCB SCHEMATIC
10/1/80	2	WIN DISC CONT	10/1/80	2	WIN DISC CONT
10/1/80	3	2013800	10/1/80	3	2013800
10/1/80	4	2013800	10/1/80	4	2013800
10/1/80	5	2013800	10/1/80	5	2013800
10/1/80	6	2013800	10/1/80	6	2013800
10/1/80	7	2013800	10/1/80	7	2013800
10/1/80	8	2013800	10/1/80	8	2013800

REV	DATE	DESCRIPTION	APPROVED
1		REVISED	
2		REVISED	
3		REVISED	
4		REVISED	
5		REVISED	
6		REVISED	
7		REVISED	
8		REVISED	



8400000-001

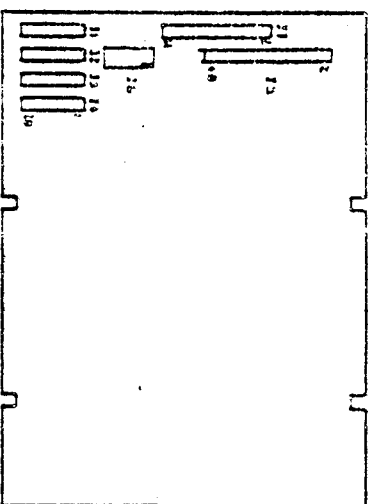
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3		REVISED	
4		REVISED	
5		REVISED	
6		REVISED	
7		REVISED	
8		REVISED	

PCB SCHEMATIC
WIN DISC CONT

REV	DATE	DESCRIPTION	APPROVED
1		REVISED	
2		REVISED	
3		REVISED	
4		REVISED	
5		REVISED	
6		REVISED	
7		REVISED	
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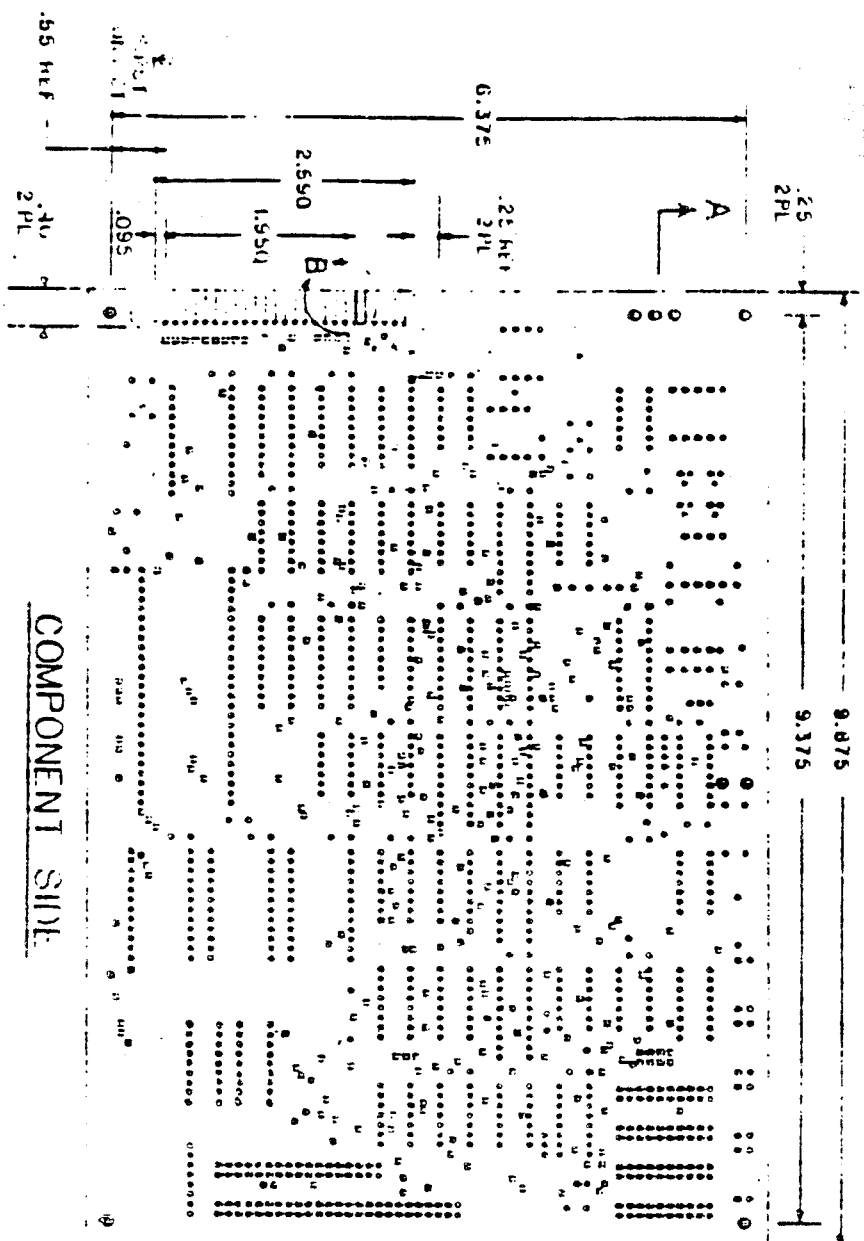
[illegible]

1	WDRF	ADDRESS, MARK, SELECT
2	AT-AD	TESTING ADDRESS SELECT, BITS 0-3
3	BOX	BUS INPUT CONTROL
4	ECEN	BUS OUTPUT CONTROL
5	DATA-DAI	CLOCK DATA
6	LIMIT-CON	ERROR CHECK/CONNECTION WORD INITIALIZE
7	CHOLD	CARD SELECT
8	OLDAY	CARD ACCESS LIMIT
9	ORF	DIRECTION CONTROL
10	SELECT	DATA HOLD
11	SRST	DELATED DATA
12	DR-DR-DRY	DATA REQUEST
13	DRUN	DATA REQUEST CLOCK
14	MRAD	DRIVE SELECT
15	MRQC	DRIVE SELECT, BITS 0-9
16	CSAC	DATA RUM
17	MSB-MS2	HIGH FREQUENCY
18	1A0-1A9	HOST ACCESS CONTROL
19	100-1015	CARD SELECT ACCESS CONTROL
20	ABIT	READ SELECT, BITS 0-8
21	ABTC	INSTRUCTION ADDRESS LMS, BITS 0-6
22	INTAG	INSTRUCTION DATA, BITS 0-15
23	102-101	HOST BUS FROM DRIVE
24	103-104	INTERUPT CLOCK
25	105-106	INTERUPT REQUEST
26	107-108	I/O TIME, 0-3
27	109-110	MISSAUF VECTOR AND, BITS 0-3
28	111-112	MASTER CLOCK
29	113-114	MODIFIED FREQUENCY MODULATION WRITE STREAM
30	115-116	MASTER SELECT
31	117-118	OSCILLATOR OUTPUT
32	119-120	BUS ADDRESS, BITS 0-9
33	121-122	READ CLOCK
34	123-124	READ CHIP SELECT
35	125-126	READ DATA
36	127-128	READ COMMAND LMS
37	129-130	READ FRAME
38	131-132	READ ADDRESS FROM DRIVE
39	133-134	READ STATUS FROM DRIVE
40	135-136	READ SIGNAL
41	137-138	READ DATA
42	139-140	DATA OUTFLOW
43	141-142	BRIDGE WRITE CURRENT
44	143-144	WRITE COMPLETE STATUS (MODE 0000)
45	145-146	STRAP
46	147-148	STEP PULL TO DRIVE
47	149-150	
48	151-152	
49	153-154	
50	155-156	
51	157-158	
52	159-160	
53	161-162	
54	163-164	
55	165-166	
56	167-168	
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441		



NOTES: WIRESS DIMENSION SPECIFIED
[1] RESISTOR VALUES ARE IN OHMS
F.B./V.M.

[illegible]

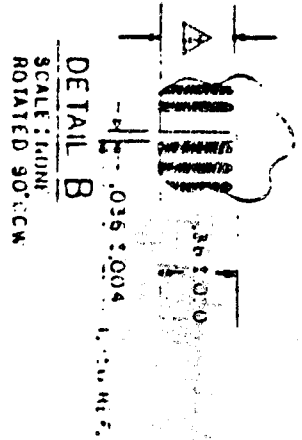


COMPONENT SIDE

HOLE LEGEND			
SYMBOL	DIAMETER FRACTION	QTY.	COMMENT
□	0.10 ± 0.03	305	
○	0.14 ± 0.03	199	
⊙	0.04 ± 0.03	2	
●	0.06 ± 0.03	3	
⊕	0.06 ± 0.03	4	100 PLATING

SECTION A-A

COMPONENT SIDE
SOLDER SIDE



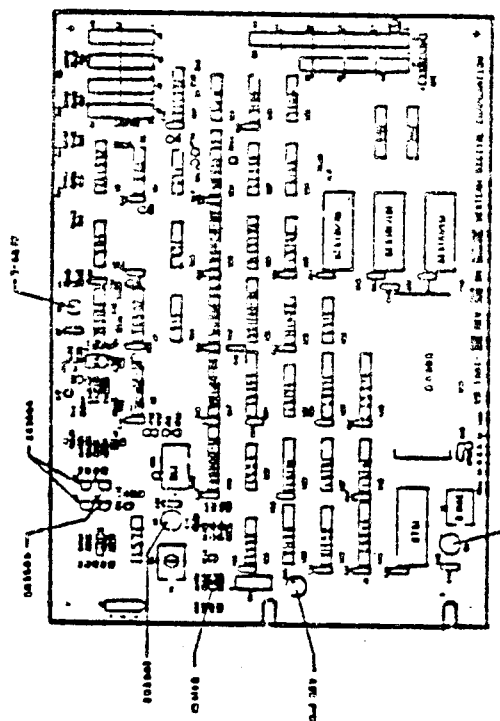
BOARD DIMENSIONS

8. SIKKSCREEN COMPONENT SIDE USING WHITE INK.
7. CONNECTOR AREA TO BE ELECTROLYTICALLY PLATED WITH 50 MIL. MINIMUMS GOLD OVER 500 MICHINCHES NICKEL.
6. SOLDER PLATE ALL EXPOSED COPPER WITH SN60.
5. SOLDER MASK BOTH SIDES OVER BARE COPPER.
4. HOLES TO BE LOCATED WITHIN .010 TRUE POSITION.
3. FRONT TO BACK REGISTRATION TO BE WITHIN .005 IN.
2. HOLES TO BE PLATED THRU TO A MIN. THICKNESS OF .001 IN.
1. MATERIAL: FL-147N 083C-1/1-A1A

NOTES:

B0 3BL		NEW DESIGN RELEASE		SY	7/27/82
A0 361		PRE-PRODUCTION		SV	5/23/82
REV ECO		DESCRIPTION		BY	DATE
REV 001		SIGNATURE		BY	DATE
REV 002		DATE		BY	DATE
REV 003		DATE		BY	DATE
REV 004		DATE		BY	DATE
REV 005		DATE		BY	DATE
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REV 096		DATE		BY	DATE
REV 097		DATE		BY	DATE
REV 098		DATE		BY	DATE
REV 099		DATE		BY	DATE
REV 100		DATE		BY	DATE

JUMPER LIST			
FROM	TO		TIME
11-9	11-12		1.5
11-10	11-13		1.5



2. GIVE A3 TO R2 ONLY AFTER R2B HAS PASSED DYNAMIC EXERCISE TEST.

3. SOLDER PIN 2 TO PIN 3 ON R3

4. ALL CAPS ARE 1/4 WATT 5% OTHERWISE SPECIFIED.

5. J1 TO BE USED FOR ST504 DRIVE

6. J2 TO BE USED FOR SA1000 DRIVE

7. R1-1000 OHM WATT FOR ST504 DRIVE

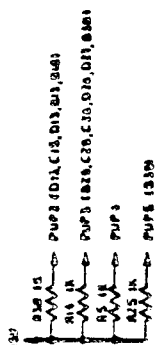
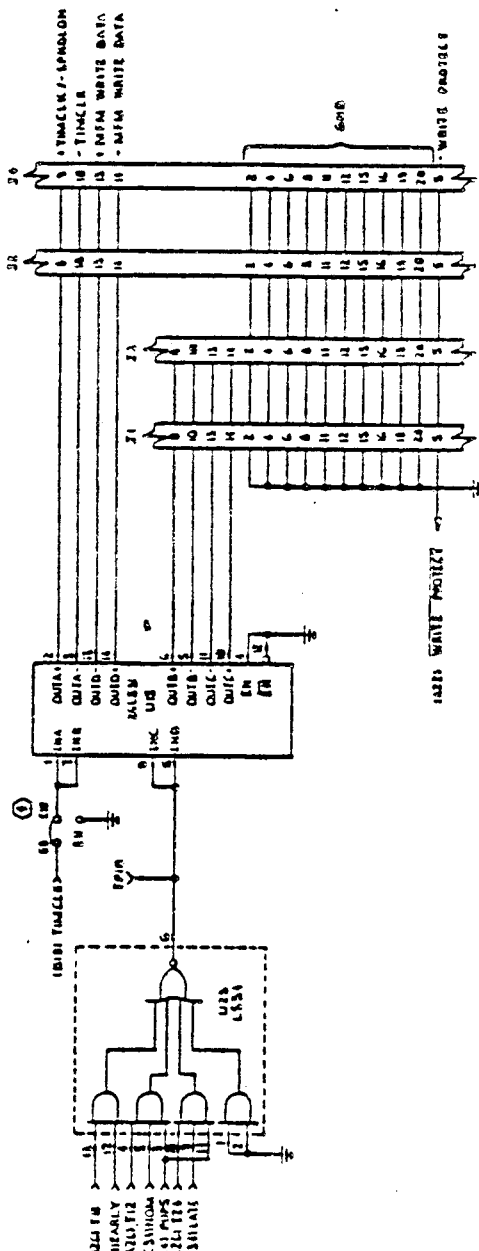
8. R1-11350 OHM WATT FOR SA1000 DRIVE

NEW BORN RELEASE
ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED
DATE 01-10-1980 BY 60322 UCBAW/STP

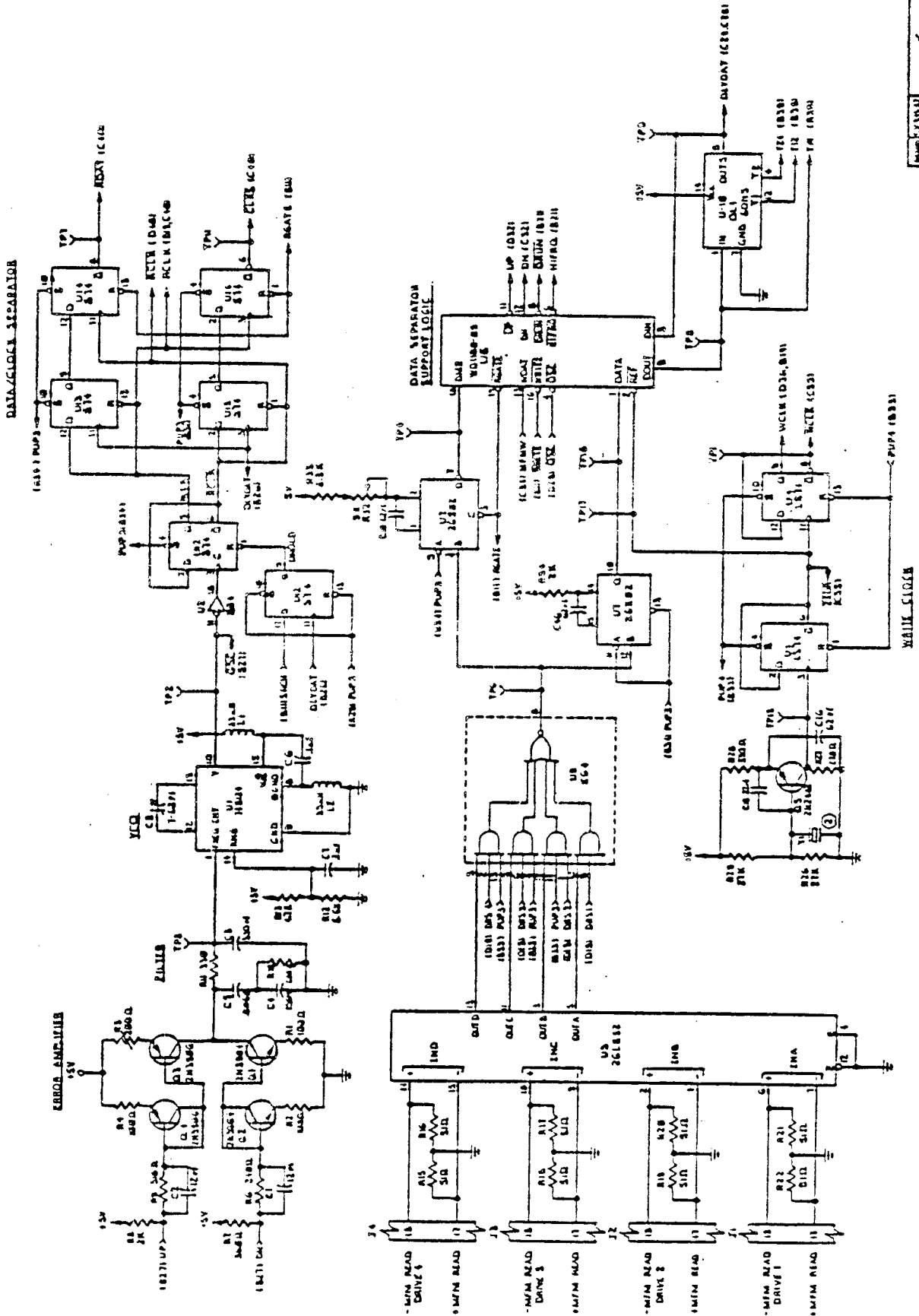
WESTERN DIGITAL
100 WESTERN AVENUE
SANTA ANA, CALIF. 92701
TEL. (714) 261-1010

DATE 01-10-1980 BY 60322 UCBAW/STP

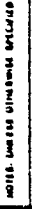
ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED
DATE 01-10-1980 BY 60322 UCBAW/STP

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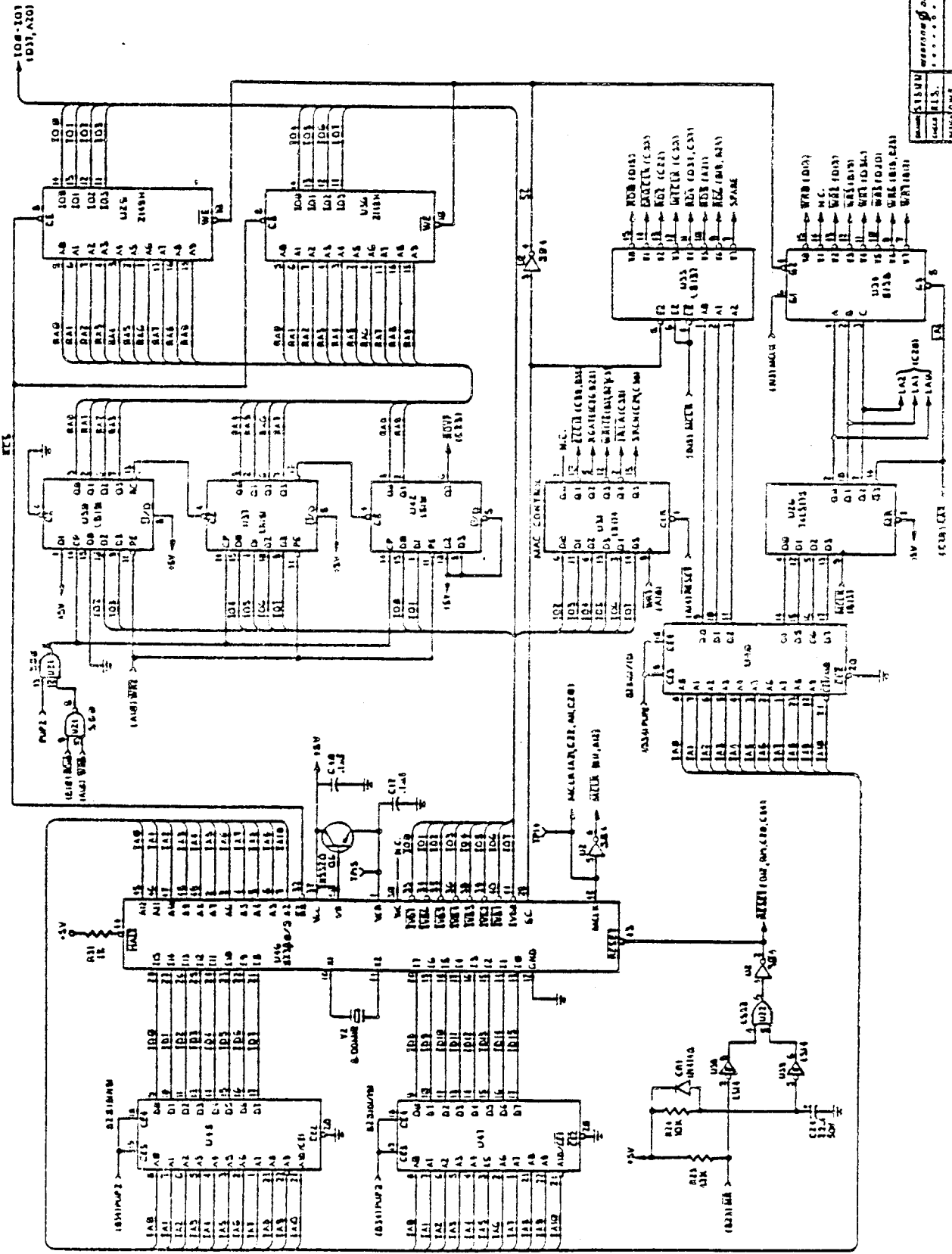
DATA SEPARATOR



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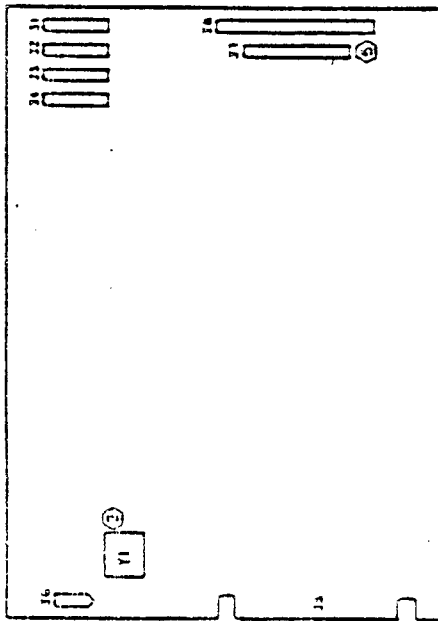
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MICROCONTROLLER



NAME	DATE	TIME	NO.
PROJECT	10/10/10	10:10	10
DESIGNER	10/10/10	10:10	10
REVIEWER	10/10/10	10:10	10
APPROVED	10/10/10	10:10	10

WD1001-55 AND WD1001-85 SCHEMATIC



NOTES: UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES ARE IN OHMS.

10	25K-100K OHM FOR ST50C DRIVE
11	25K-100K OHM FOR ST50C DRIVE
12	10-100K OHM FOR ST50C DRIVE
13	10-100K OHM FOR ST50C DRIVE
14	10-100K OHM FOR ST50C DRIVE
15	10-100K OHM FOR ST50C DRIVE
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99	10-100K OHM FOR ST50C DRIVE
100	10-100K OHM FOR ST50C DRIVE

ONLY IN OPERATION

ANALYST	ADDRESS MARK DETECT
AT-AB	TASK FILE ADDRESS SELECT, BITS 0-2
ATC	BUS INPUT CONTROL
ATC	BUS OUTPUT CONTROL
CLIPS	CLOCK DATA
CLIPS	CARD CHECK/CONNECTION WARD INITIALIZ
CLIPS	CARD SELECT
CLIPS	DATA ACCESS LINES
CLIPS	DIRECTION CONTROL
CLIPS	DATA HOLD
CLIPS	DELATED DATA
CLIPS	DATA REQUEST
CLIPS	DATA REQUEST CLOCK
CLIPS	DATA SELECT
CLIPS	DATA SELECT, BITS 1-9
CLIPS	DATA RUN
CLIPS	HIGH FREQUENCY
CLIPS	HOLD ACCESS CONTROL
CLIPS	CARD SELECT ACCESS CONTROL
CLIPS	HEAD SELECT, BITS 0-2
CLIPS	INSTRUCTION ADDRESS LINES, BITS 0-8
CLIPS	INSTRUCTION DATA, BITS 0-15
CLIPS	INJECT PULSE FROM DRIVE
CLIPS	INTERUPT CLOCK
CLIPS	INTERUPT REQUEST
CLIPS	I/O LINES, 0-3
CLIPS	INTERUPT VECTOR BUS, BITS 0-3
CLIPS	MASTER CLOCK
CLIPS	MODIFIED FREQUENCY MODULATION WHITE STREAM
CLIPS	MASTER SELECT
CLIPS	OSCILLATOR OUTPUT
CLIPS	RAW ADDRESS, BITS 0-9
CLIPS	READ CLOCK
CLIPS	READ DATA SELECT
CLIPS	READ DATA
CLIPS	READ CONTROL LINES
CLIPS	READ ENABLE
CLIPS	READY STATUS FROM DRIVE
CLIPS	READY SIGNAL
CLIPS	READ GATE
CLIPS	RAM OVERFLOW
CLIPS	REDUCE WHITE CURRENT
CLIPS	SEEN COMPLETE STATUS FROM DRIVE
CLIPS	SEARCH
CLIPS	STEP PULSE TO DRIVE
CLIPS	TIME CLOCK SIGNAL FROM LAUNCH
CLIPS	TRACK 0-9 STATUS FROM DRIVE
CLIPS	WAIT ENABLE
CLIPS	MEMORY NOT READY SIGNAL
CLIPS	WHITE CLOCK
CLIPS	WHITE ENABLE
CLIPS	WHITE GATE INTERNAL
CLIPS	WHITE STATUS FROM DRIVE
CLIPS	WHITE CONTROL LINES
CLIPS	1-BYTE LOOK AHEAD
CLIPS	2-BYTE DATA REFERENCE CLOCK
CLIPS	INTERNAL UNDER SYNC SIGNAL
CLIPS	READ BYTE SYNC
CLIPS	DATA SYSTEMS DRIVE STATUS SIGNAL

[illegible]